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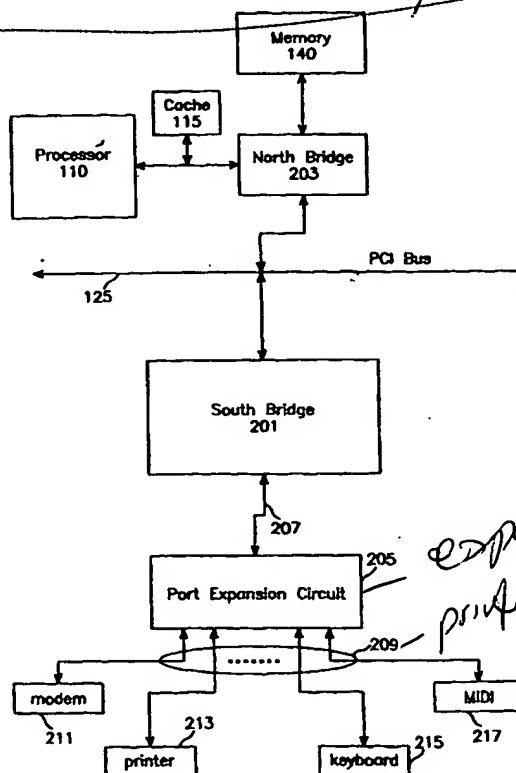
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(54) Title: SYSTEM FOR PARTITIONING PC CHIPSET FUNCTIONS INTO LOGIC AND PORT INTEGRATED CIRCUITS

(57) Abstract

A first integrated circuit includes interface logic between legacy device and an expansion bus. A second integrated circuit provides input and output terminals for the interface logic. A bus couples the first and second integrated circuits and transfers data substantially continuously between the first and second integrated circuits. The data includes output signals from the interface logic which is provided to the output terminals of the second integrated circuit and input signals for the interface logic from the input terminals of the second integrated circuit. The data is transferred between the first and second integrated circuits in frames which include a predetermined number of data bits and preassigned slots for the states of the input and output signals, so as to continuously transfer the state of the input and output signals to and from the input and output pins of the second integrated circuit at a predetermined rate. The second integrated circuit includes input/output terminals to couple to legacy devices such as a keyboard, a mouse, a game port, a musical instrument digital interface (MIDI) port, a floppy drive, a PC speaker and an infrared port.



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SYSTEM FOR PARTITIONING PC CHIPSET FUNCTIONS INTO LOGIC AND PORT INTEGRATED CIRCUITS

TECHNICAL FIELD

5 The present invention relates to computer systems, and, more particularly, to the partitioning of input/output functions among integrated circuits.

BACKGROUND ART

10 A typical personal computer (PC) system includes a microprocessor, associated memory and control logic and a number of peripheral devices that provide input and output for the system. Such peripheral devices typically include a display monitor, a keyboard and mouse, a floppy disk drive, a hard disk drive and a printer. The number of devices being added to personal computer systems continues to grow. For example, many computer systems also include modems, sound devices, and CD-ROM drives.

15 PC systems use one of several expansion bus architectures to facilitate communication between various components of the system and to provide the versatility needed to add additional components to the system. For example, Industry Standard Architecture (ISA) provides an expansion bus for the 16-bit IBM AT personal computer. The Enhanced ISA (EISA) provide specifications for systems utilizing 32-bit microprocessors such as the Intel 80386 and 80486 microprocessors. The Peripheral Component Interconnect (PCI) bus provides a bus architecture for 32-bit or 64-bit interconnection systems independent of processor generation or family.

20 The ISA bus, originally called the Advanced Technology (AT) bus, added the functionality needed for full 16-bit technology, but maintained compatibility with an older 8-bit PC bus. Because of its initial speed and data-path match with the 80286 microprocessor, the original ISA bus substantially out-performed the PC bus. The ISA bus has resisted replacement by newer bus architectures such as EISA and Microchannel, and remains commonplace in personal computer systems in use today. This is true in part because many devices that are designed to interface with the ISA bus are in widespread use today. Such devices typically do not require the higher speed provided by the newer buses. Such devices are known as legacy devices since their design is based on older PC technology. Examples of such slower legacy devices include keyboards, and mouse(s), game ports, and floppy drives, modems and printers connected respectively to serial and parallel communication ports, direct memory access (DMA) controllers, interrupt controllers and timers. Those legacy devices do not need the high speed throughput of the newer generation of buses such as EISA, Microchannel Architecture (MCA) and the Peripheral Component Interface (PCI) bus.

30 Although personal computer system speeds have increased dramatically, the speed of the ISA bus is limited to 8 MHz. As higher speed processors were utilized, dedicated memory buses were added to personal computer systems because the ISA bus was too slow for the required high speed memory accesses. Video

applications also became limited by the bandwidth of the ISA, so systems began to use a "local bus" for video applications. Although initially targeted at advanced video systems, new local bus specifications were made broad enough for handling other peripherals requiring high-bandwidth transfers such as mass storage devices and network interfaces.

5 The Peripheral Component Interconnect (PCI) bus is one example of a local bus specification. The VL bus is another local bus specification that has been less widely adopted. The PCI bus provides a high-speed interconnection system which runs more closely to microprocessor speeds than does a traditional expansion bus. And, although initially designed for 32-bit microprocessors, the PCI specification is broad enough to include the 64 bit data paths of the advanced processors. Legacy devices compatible with older bus
10 architectures such as ISA connect to the PCI bus via a bus bridge circuit.

Many present day personal computer systems contain both a PCI bus and an ISA bus. The PCI bus is used to connect to newer peripherals and/or those peripherals requiring a higher speed interface. The ISA bus is typically connected to legacy devices. Historically, interfaces to peripherals utilized a large number of discrete components. However, the levels of integration has continued to increase in PC systems. As a result,
15 much of the functional logic which is required to interface with peripheral devices has been integrated into a relatively few integrated circuits (ICs) which are sold as chip sets for the PC. The ICs include a plurality of terminals, pins, or leads, connecting the IC to the printed circuit board (PCB) to which the IC is mounted. The PCB functions as a system board. The terminals communicate input/output (I/O) signals between one IC and other ICs or I/O devices coupled to the system board. These system boards often receive expansion PCBs to
20 increase the capabilities of the computer system and to connect to peripheral devices, e.g., through the ISA bus.

Referring, to Figure 1, an exemplary prior art computer system 100 is shown conforming to the above architectural approach of including both a PCI bus and an ISA bus. Computer system 100 includes processor 110 which is coupled to secondary cache 115 and memory 140. Bridge 120 provides an interface
25 between the processor/memory system 105 and PCI bus 125. Bridge 120 provides a communication link between PCI devices 150, 160 and 170 and the processor/memory system 105. In fact, although the PCI bus was originally intended for graphics, high speed graphics requirements have resulted in another specialized graphics bus called the Advanced Graphics Port Bus which can be utilized in place of the PCI bus for graphics applications. The PCI devices may be integrated circuits on the system board of computer system 100,
30 expansion components connected to PCI bus 125 via expansion slots, or some combination thereof. A second bridge 130, provides a bus interface between the PCI bus 125 the ISA expansion bus 135. In order to communicate with legacy devices which are designed to interface to the ISA bus, one approach, consistent with the trend towards increased integration in the PC, has been to provide Super I/O chip 170 rather than provide a number of discrete interfaces.

Super I/O chip 170 provides I/O terminals and control logic for commonly used legacy peripheral devices such as keyboards, IDE drive, IEEE parallel port, serial communication ports. One example of such a Super I/O chip is the National Semiconductor PC87306 Super I/O chip. Thus, legacy devices can be included in the system by utilizing the bridge 130, the ISA bus, and Super I/O chip 170.

5 DISCLOSURE OF INVENTION

It has been discovered to combine a bridge function such as a PCI bridge with a Super I/O function. Further, it has been discovered to provide a first integrated that includes super I/O functional logic to logically interface to legacy devices and a second integrated circuit that provides the input/output terminals for the super I/O functional logic to physically interface to legacy devices.

10 Accordingly, the invention provides a first integrated circuit that includes functional logic and a second integrated circuit which provides input and output terminals for the functional logic. A bus couples the first and second integrated circuits and transfers data substantially continuously between the first and second integrated circuits. The data includes output signals from the functional logic which is provided to the output terminals of the second integrated circuit and input signals for the functional logic from the input terminals of
15 the second integrated circuit.

The data is transferred between the first and second integrated circuits in frames, each frame includes a predetermined number of data bits and each frame includes predetermined slots for the states of the input and output signals, so as to continuously transfer the state of the input and output signals to and from the input and output pins of the second integrated circuit at a predetermined rate. During a power conservation mode,
20 the bus stops transferring data. The functional logic in the first integrated circuit includes an input/output bus conforming to an industry standard architecture (ISA) and a plurality of ISA interfaces coupled to the input/output bus, the interfaces providing an interface between the input/output bus and a plurality of devices. The second integrated circuit includes input/output terminals to couple to a at least one legacy device wherein the at least one legacy device is one of a serial port and a keyboard and a mouse and a game port and a
25 musical instrument digital interface (MIDI) port and a floppy drive and a PC speaker and an infrared port.

Such a system provides the advantages of combining the bridge function and the super I/O function. Additionally, the invention allows incorporating the ISA bus into the bridge chip. The separation of the functional super I/O logic and the I/O terminals into the first and second integrated circuit, respectively, also alleviates the pressure on pin count and package cost. As more and more functions are integrated into an IC,
30 more I/O pins are required. The greater the pin count, the greater the package cost. A combined bridge and super I/O function requires providing I/O for the PCI bus as well as the large number of I/O terminals required to support the legacy devices. Separating the logic and I/O function into separate integrated circuits reduces the pressure on pin counts and package cost.

IC

The invention also provides the advantage of avoiding problems associated with reduced supply voltages. As process geometries shrink, supply voltages drop, e.g., to 3.3 volts or less, leading to problems interconnecting to the various super I/O interface pins. The super I/O typically drives legacy devices having 5 volts I/O logic. The smaller geometries utilized for today's faster and denser integrated circuits can have problems interconnecting at that voltage. The invention provides for building the first integrated circuit with the smaller process geometries to provide a faster and denser chip. However, the second integrated circuit can be built with slower technologies, e.g., where the transistors have channel lengths of 0.5 microns or above. Thus, the problem of connecting 5 volts legacy interfaces to integrated circuits made with smaller process geometries is also reduced.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings, wherein the use of the same reference symbols in different drawings indicates similar or identical items.

Figure 1 shows a schematic block diagram of a prior art personal computer.

15 Figure 2 shows a block diagram of a PC which includes a South Bridge circuit and port expansion circuit in accordance with the present invention.

Figure 3 shows a block diagram of the South Bridge circuit of the personal computer architecture of Figure 2.

20 2. Figure 4 shows a block diagram of a port expansion circuit (PEC) of the personal computer of Figure 2.

Figure 5 shows a four line embodiment of the bus connecting the South Bridge and the port expansion circuit of the personal computer of Figure 2.

Figure 6 is a timing diagram for the port expansion bus (PEB).

25 Figure 7 is a timing diagram showing the relation between the frame sync signal, the bit clock, Data In and Data Out on the port expansion bus.

Figure 8a shows the frame transmitted from the South Bridge to the port expansion circuit on Data Out.

Figure 8b shows the frame transmitted from the port expansion circuit to the South Bridge on Data In.

Figure 9a is a schematic block diagram of the port expansion bus host interface in the South Bridge.

Figure 9b is a schematic block diagram of the receive logic of the port expansion bus host interface in the South Bridge.

Figure 10 is a schematic block diagram showing further details of the port expansion circuit.

5 Figure 11 shows a six line embodiment of the port expansion bus.

Figure 12a shows the frame transmitted from South Bridge to the port expansion circuit on Parallel Data Out for Standard/PS2 mode on the parallel port.

Figure 12b shows the frame transmitted from the port expansion circuit to South Bridge on Parallel Data In for Standard/PS2 mode on the parallel port.

10 Figure 13a shows the ECP mode bit assignments in the frame transmitted to the port expansion circuit from South Bridge.

Figure 13b shows the ECP mode bit assignments in the frame transmitted from the port expansion circuit to South Bridge.

15 Figure 14a shows the EPP Write mode bit assignments in the frames sent to and received from the port expansion circuit.

Figure 14b shows the EPP Read mode bit assignments in the frames sent to and received from the port expansion circuit.

Figure 15 shows a game port configuration which includes two joysticks.

20 Figure 16 is a schematic block diagram of the circuit that determines the X or Y position of the joystick.

Figure 17 is a timing diagram illustrating the functioning of the circuit in Figure 14a.

Figure 18 illustrates an example of the use of the general I/O and the PLA on the port expansion circuit.

25 Figure 19 is a timing diagram illustrating restarting of the port expansion bus from a power-down condition.

MODE(S) FOR CARRYING OUT THE INVENTION

Figure 2 shows a personal computer system according to the present invention. The personal computer system comprises processor 110 which is coupled to cache memory 115 and memory 140. Bridge circuit 203 (North Bridge), provides an interface between the processor and memory and the PCI bus 125.

5 Bridge circuit 201 (South Bridge) provides an interface between PCI bus 125 and a plurality of legacy devices. The bulk of the I/O pins that would normally be required to provide I/O for the South Bridge are provided instead on a separate circuit 205, connected to the South Bridge 201 via port expansion bus 207. The separate circuit 205 will be referred to herein as the port expansion circuit (PEC). The port expansion circuit provides I/O 209 to connect to the plurality of legacy devices such as a modem 211, a printer 213, a keyboard and/or

10 mouse 215 or an electronic instrument 217 through a Musical Instrument Digital Interface (MIDI). The port expansion bus 207 connecting port expansion circuit 205 and South Bridge 201 operates to transfer signals that should be output to the legacy devices from the South Bridge to the port expansion circuit 205. The port expansion bus 207 also operates to transfer signals that are received from the legacy devices from the port expansion circuit to the South Bridge. In a preferred embodiment, both the South Bridge 201 and the

15 port expansion circuit 205 are each separate integrated circuits.

Additional legacy devices are also supported by the South Bridge in combination with the port expansion circuit and will be described further herein. The South Bridge includes the logic necessary to interface the legacy devices to the rest of the computer system through the ISA bus. In addition to the I/O function, the port expansion circuit may incorporate additional logic functions as described further herein.

20 Referring now to Figure 3, the South Bridge is shown in greater detail. Specifically, the South Bridge includes a number of logic blocks to support interfacing the most commonly used legacy I/O devices. For instance, in a preferred embodiment, the South Bridge may include one or more universal asynchronous receiver transmitter(s) (UART) block 309, which for the embodiment shown is a 16550 UART, an infrared (IR) interface block 311 which may support both the Infrared Data Association (IrDA) standard and the Fast

25 IR standard, Programmable Interval Timer (PIT) 312 which couples to the PC speaker on the port expansion circuit side., a parallel interface controller 313 for the IEEE 1248 parallel port, interface logic 315 for the keyboard and for the mouse, interface logic 317 for the game port, interface logic 318 for a MIDI port and General I/O 319 which is described further herein. A floppy controller 321 is also provided. Note that in some

30 embodiments the floppy controller may include some input/output pins on the South Bridge and in other embodiments all the input/output pins are on the port expansion circuit. When the data separator is on the port expansion circuit, all the pins can be reflected onto the port expansion circuit and the I/O 322 coming off the South Bridge becomes unnecessary.

Those logic blocks to logically interface the legacy devices are coupled to ISA bus 307 which is internal to the South Bridge. Thus, in one preferred embodiment, the ISA bus has been incorporated into the

35 South Bridge chip and the legacy devices are devices that interface to the ISA expansion bus (input/output

bus) through the interface logic in the South Bridge. ISA bus 307 is coupled through ISA Bridge 325 to Gen Bus 327 which in the embodiment shown is a simplified PCI bus. In turn, Gen Bus 327 is coupled through interface block 329 to the PCI bus 125. The South Bridge also includes sideband signals 329 which are coupled to the North Bridge. Such sideband signals provide for legacy signals such as interrupts which can not be handled over the PCI bus.

Each of the functional blocks 307-321 provide the logic necessary to interface signals from the ISA bus 307 to each of the devices coupled to the port expansion circuit. For example, block 309 which is a 16550 UART can be connected to a serial communications device such as a modem. Block 313 may be connected to a printer or other device on the parallel port. The floppy control block 321 is coupled to a floppy drive and the game port can be coupled to two joysticks. The keyboard and mouse control block 315 can be coupled to a keyboard and/or a mouse. The function of the control blocks 307-321 in the South Bridge to interface to the legacy devices is well known and the detailed functioning of that logic will not be further described except when needed for a better understanding of the claimed invention. All these blocks require I/O connectors to provide signals to and receive signals from the various legacy devices to which they are provide a logic necessary for interfacing to the ISA bus.

Providing I/O capability for all the legacy devices as well as performing the bus interface and other functions on the South Bridge would require an IC with more I/O capability and would therefore could be a more expensive part. It is preferable to build an IC which can be more inexpensively packaged in, e.g., quad flat packs and avoid more expensive packaging such as ball grid arrays which can provide higher pin density but can also be more costly to produce. In many instances, reducing pin count significantly can reduce the package cost of the product.

Separating the I/O function from the logic function provides further advantages. As discussed, as process geometries shrink for faster and denser integrated circuits, e.g. channel lengths of 0.35 microns and below, supply voltages drop, e.g., to 3.3 volts or less, leading to problems driving the various devices on the super I/O interface pins which are typically 5 volts. The super I/O interfaces tend to be 5 volts interfaces which is typical of the legacy devices. Since high speed is desired for the South Bridge IC, it is preferable to build the chip with the smaller process geometries to provide a faster and denser chip. However, the port expansion circuit chip can be built with slow technologies, e.g., where the transistors have channel lengths of 0.5 microns or above. That allows the port expansion circuit to be built with older and less expensive process technology and also allows the port expansion circuit to easily interconnect to the 5 volts interfaces typical of the legacy devices. At the same time, the more speed sensitive South Bridge can be built with the most up to date process technologies providing channel lengths for the transistors of the internal logic of, e.g., 0.35 microns, without the problem of interconnecting to a large number of 5 volts interfaces.

Therefore port expansion circuit 205 provides the I/O terminals for the logic block 309-321 for coupling the logic block 309-321 pins to the devices. That entails sending the output signals from the South

Port
Expansion

Bridge to the port expansion circuit at a rate that is faster than the rate of change of the signals that are sent. Further, the input signals on the connectors of the port expansion circuit must be sent to the logic interfaces in the South Bridge for the particular device, such as a modem, at a rate faster than the rate of change of the signals from the particular device.

5 Each of the blocks 309-321 in the South Bridge are coupled to interface logic 323 also called the Port Expansion Bus host. The port expansion bus host interface 323 is also coupled to Gen Bus 327 Bus 207 so that the CPU can read and write certain registers in the host interface as described further herein. Note that the host interface 323 may be coupled to ISA bus 307 instead of Gen Bus 327.

10 Bus 207, which will be referred to herein as the Port Expansion Bus (port expansion bus), couples host interface logic 323 to the port expansion circuit 205. port expansion bus 207 is utilized to transfer the states of the output signals from the functional blocks 309-321 to the output pins of the port expansion circuit. port expansion bus 207 is also used to transfer the states of the signals on the input pins of the port expansion circuit to the appropriate blocks in the South Bridge.

15 The port expansion circuit 205 is shown in block diagram form in Figure 4. The port expansion bus target interface 403 provides the interface to port expansion bus 207. Interface 403 provides signals from the South Bridge IC to the output pins for serial ports 405, PC speaker 407, parallel port 409, keyboard and mouse 411, game port 413, MIDI port 415, floppy 417, IR port 425 and General I/O 419. Control block 421 provides control function for interface 403. For example, control block 321 also provides a power management function which is discussed further herein. In addition, the control block decodes commands sent from the South Bridge and maintains status information which can be provided to the South Bridge as discussed further herein. Clock synthesizer 421 provides the multiple clocks which are required by the PC system. The clock synthesizer is also discussed further herein.

20 In order for the Port Expansion Circuit 205 to provide I/O function for the South Bridge IC, the output signals from the interface logic blocks in the South Bridge IC have to be reflected onto the output pins of the port expansion circuit. Therefore, the output signals have to be sampled in the South Bridge and provided to the output pins of the port expansion circuit at a rate faster than the output signals change. Additionally, the input signals on the input pins of the port expansion circuit have to be sampled and provided to the interface logic blocks in the South Bridge IC at a rate faster than the input signals change. In one exemplary embodiment, a protocol-free six wire bus running at about 50 MHz provides the necessary bandwidth to allow the port expansion circuit to provide I/O for the various interface logic blocks in the South Bridge. Utilizing such an approach can reduce the South Bridge pin count by approximately 70 or more pins. Such savings in pin count generally leads to a less costly chip.

30 The bus comes in several preferred embodiments. In a first embodiment, which is intended to provide pin reflection capability for slower devices, the bus is a basic four-pin serial bus shown in Figure 5. A second embodiment of the bus is provided in order to support higher speed ports, e.g., to provide the necessary

bandwidth for the higher speed parallel port. In some circumstances, only the first embodiment may be necessary, if for instance, the parallel port is not utilized or is connected to the South Bridge rather than the port expansion circuit, or if the speed of the port expansion bus is increased significantly.

5 Referring now to Figure 5, the first embodiment of the bus includes a frame sync 501 and a synchronous data clock 507 and a Data In line 505 (data from the port expansion circuit to the South Bridge), and Data Out line 507 (from the South Bridge to the port expansion circuit). In the exemplary embodiment, the nominal clock rate is 50 MHz and a frame is chosen to contain 96 bits. Other frame lengths and clock rates are of course possible.

10 Referring to Figure 6, the beginning of each frame is determined by assertion of the frame sync signal. The frame sync signal is preferably a 50% duty cycle signal to facilitate counting frame bits. Other duty cycles are of course possible. One frame consists of 96 clock periods. Referring to Figure 7, one data bit is provided on the Data Out and Data In line each clock period during each frame. The data bits are provided relative to the rising edge of the bit clock in the embodiment shown. With a frame of 96 bits, the frame rate is nominally 500 kHz. Each bit in each frame that represents an I/O bit is sampled and provided from/to the
15 appropriate I/O pin of the port expansion circuit approximately every 2 microseconds. That speed is sufficiently high to support most of the legacy devices supported by the port expansion circuit.

In order to help ensure that the interfaces to the legacy devices operate correctly, i.e., that the I/O signals are adequately reflected, in a preferred embodiment, the bus is "protocol free," in that there are no activation sequences or complex state machines required. The bus is simply a 96-bit time-slot structure where
20 each bit time is assigned a specific function. Figures 8a and 8b show the non-parallel port bit time slot assignments to and from the port expansion circuit. All bits in Figures 8a and 8b are numbered with respect to the leading edge of frame sync. In addition to being "protocol free", the bus operates to continuously transferring frames between the port expansion circuit and the South Bridge. The frames are contiguous in that there is no time between each frame, i.e., the start of bit 0 is one clock period from the start of bit 95.
25 However, other embodiments may provide some time periods between frames so long as the port expansion bus stays substantially continuously running to sufficient to satisfy the speed requirements of the pin reflection approach described herein. The I/O pin values are transferred every 2 microseconds whether they change or not. However, the bus does not operate while the port expansion circuit and South Bridge are in a power down mode to reduce power consumption..

30 Referring again to Figures 8a and 8b, the frame includes provision (Link Command/ Status) for transmitting commands to the Port expansion circuit (port expansion circuit) and receiving back status from the port expansion circuit. Commands are transmitted from the South Bridge to the port expansion circuit via the first nine bits of the frame. Bit 0 is a flag that, when set, indicates that the command field is valid and therefore a new command is being transmitted. Bits (1:8) contain the command byte – thus there are 256
35 possible commands. The individual commands can be, for example, requests for the port expansion circuit to

take some action (such as entering a power management state) or a request to read a register within the port expansion circuit.

Commands are sent only once. That is the Valid bit (bit 0) is only active for a single frame.

Commands are transmitted during the next frame following a CPU write to the port expansion circuit Link

5 Command Register 901 which is located in the host interface in the South Bridge as shown in Figure 9a.

There is no provision for buffering up commands. A Command Buffer Empty status bit 903 is provided in the South Bridge indicating that a new command can be sent.

10 When the Valid bit (bit 0) is inactive, the link command bits 0-7 may be used to transfer other information such as static command information. Such static command information may include a "keep alive" field which informs the port expansion circuit that the South Bridge is still present.

15 In the receive frame received from the port expansion circuit, the bits corresponding to the link command bits in the transmit frame are link status bits (bits 1:8). The status field has two modes. First, the status field presents static status information, i.e., the eight bits reflect the current status of the port expansion circuit. The static status field may include such information as the mode of the parallel port, the mode in which other ports are operating, the power mode of the port expansion circuit and any diagnostic information available. Secondly, the status field can be used to return read data requested by the a specific command sent from the South Bridge, i.e., a command sent from the South Bridge in the Link Command field requesting that specific data, such as the contents of a register be returned. The Response/Status bit (bit 0) indicates which mode the link status field is operating in during that frame.

20 When the Response/Status bit is active, the data field (bits 1:8) contains the response to a request received in the immediately preceding frame. Responses are only sent for a single frame time. Referring to Figure 9b, there is only a single byte buffer 907 (the port expansion circuit Response Register) for received responses located in the South Bridge.. User software should not transmit additional response requests until it has read the data from the port expansion circuit Response Register. A status valid bit 909 is provided
25 indicating the availability of valid data in the port expansion circuit Response Register for the CPU. The bit is cleared when the port expansion circuit Response Register is read. Static status information is transmitted during all frames where the Response/Status bit is non asserted.

30 With the exception of the link command/status field, printer port data fields, game port X and Y comparators, and reserved bits, all bit positions in the frame are "reflected pins." In essence, the state of a signal on the transmitting side of the link is reflected to a signal on the other side. The state of each bit is updated each frame time (nominally every 2 microseconds). In this way, the states of relatively slow changing signals can be transmitted over a time-division serial bus and recreated on the other side. The state of input pins on the port expansion circuit are sent to the South Bridge via the Data In pin. The state of output pins on the port expansion circuit are sent from the South Bridge via the Data Out pin.

Referring again to Figures 9a and 9b, the port expansion bus host interface 323 in the South Bridge is shown in greater detail. The various bits located at the outputs of the logic interface blocks 309-321 are provided to multiplexing logic block 910. The correct bit is selected for output onto Data Out line 503 at the right time slot based on the value in the counter 912. Decodes of the counter value is used in decode logic 914 to select the appropriate bit to output at the particular time slot. In one embodiment, output register 916 may be implemented as a serial shift register, that is loaded up every 8 bit clocks with new data to be shifted out.

Figure 9b shows additional details on the receive side of the host interface 323. Data In is received on the Data In line 505 from the port expansion circuit and placed in the input register 920. In some implementations, register 920 may be a single bit and in other implementations, it may be a serial shift register which buffers, e.g., a byte of data before the data is provided to the appropriate logic interfaces. The decode logic 922 which directs the input data through logic 924 to the appropriate ports, e.g. port 315-318, may have significant overlap with decode logic 914 shown in Figure 9a. When a bit is received, it is transmitted to the appropriate interface and clocked into the input port of that interface. That function may be accomplished by enabling a clock to that input latch when the time slot for that bit has been received.

Figure 10 shows additional details of the port expansion circuit. Data is received on Data Out line 503 from the South Bridge. It is received into a data register 1001 and sent to the appropriate I/O port 405 through 419 based on the counter value in counter 1003 and decode logic 1007 and logic 1011. Logic 1011 may provide a clock to the appropriate output port at the appropriate bit time. The control logic 421 includes the command decode logic 1005 to decode commands sent from the South Bridge as well as status register 1009. Data bits received from the I/O ports are assigned to their correct bit times in each frame by multiplexing logic 1013 and provided to the data out register 1015 at the appropriate bit time.

An example of pin reflection according to the invention is as follows. The PC Speaker is connected to the counter-timer block 312 in the South Bridge and the frequency of the speaker is determined by the frequency of the digital signal output by the counter timer block 312 which is an 8253 or 8254-2 equivalent timer/counter. At the start of bit time 82 of each frame, the state of the counter timer's PC Speaker output is sampled. Bit position 82 in the frame transmitted to the port expansion circuit is updated to reflect the sampled state. At the port expansion circuit end, the state of the Data Out pin is latched during bit time 82. The PC Speaker pin on the port expansion circuit always reflects the latched value. Thus, the PC Speaker pin always reflects the state of the counter timer output, with a delay of up to 2 microseconds.

Functions within a personnel computer system that utilize pin reflection include and can be supported by the 4 pin bus described herein include the PC Speaker, MIDI Port, Keyboard, Mouse, Serial Ports and General I/O. The Parallel Port and the Game Port and the Floppy port may not use pin reflection for all functions.

The transmit frame shown in Figure 8a includes bits 32:42 for the floppy disk drive. Serial port 0 and serial port 1 are provided in bits 48:50 and 53:55, respectively. Bits 54 to 57 may also be used for an infrared

port such as the Infrared Data Association (IrDA) port. Bits 65:68 are utilized for the game port. Bit 82 provides the PC speaker out. Bit 83 is a MIDI transmit (TX) bit. Bits 84-95 are user defined bits. The remaining bits are reserved for future use.

The receive frame is shown in Figure 8b includes bits 32:35 as inputs from the floppy drive. Bits 48:57 are serial port 0 and serial port 1 bits. Bits 54:57 may be utilized for an IrDA port or a mouse as indicated. Bits 65:72 are utilized for the game port inputs. Bit 83 is a MIDI receive (RX) bit. As shown bits 84-95 are examples of what might constitute general I/O bits. For example, bit 84, Vol+, bit 85 Vol- and bit 86, mute, could be used to control speakers that are resident in a terminal. Bit 87 can be used as a key lock indicator indicating the status of the lock on the front of the computer. The turbo bit can indicate if the PC is in turbo mode. Setup disable can indicate the user of the PC is prevented from going into a setup mode. CLR CMOS is used to clear battery backup memory containing basic system configuration such as what drives are installed and how much memory is available. Bits 91-94 could be used to indicate the status of dip switches on the board. Bit 95 is a general I/O bit. The remaining bits in the frame are reserved for future use.

While the 500 kHz update rate is sufficient for the signals described so far, that update rate may not be fast enough for certain of the devices. For instance, the PC parallel port is capable of transferring up to 2M-bytes per second. As a result of this data rate, it is not practical to simply reflect the state of the printer port's pins across the serial bus described in the first embodiment. Thus, a second embodiment is provided.

Referring to Figure 11, the set of four pins of the first embodiment is supplemented by a second pair of data pins 1101 and 1103, Parallel Data In and Parallel Data Out, respectively, which are dedicated to the parallel port. Additional dedicated pins may be utilized for other fast devices which can not be supported by the first embodiment of the port expansion bus. The static pins are reflected in the normal way across Parallel Data In and Parallel Data Out, while the data pins and necessary timing strobes are generated within the port expansion circuit. The dedicated data pins support the different parallel port modes that are defined in the IEEE 1284 specification ("IEEE Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers"), which is incorporated herein by reference. The IEEE 1284 parallel port specification outlines a number of separate operating modes, including: (1) Standard (2) PS2 (3) Enhanced (EPP) and (4) Extended Capabilities (ECP). The Link Command field (bits 0:8) are used to specify the operating mode of the parallel port.

Briefly, these modes provide the following capabilities. In Standard mode, write-only capability is provided. That is, the parallel port may be used only to write to an external device, normally a printer. The write operation is totally controlled by CPU I/O reads and writes of command and status bits. In Standard Mode typical cycle, the CPU writes data to the parallel port data register in the South Bridge. The CPU writes the control register in the South Bridge setting bit (0) to activate the strobe (STB) pin. In response, the printer, activates the Busy pin and once the data has been processed by the printer and the printer is ready to receive the next byte of data, the printer activates the acknowledge (ACK) pin. ACK going active generates an

interrupt (IRQ) to the CPU. If more data is to be sent, then the CPU repeats the cycle by writing to the data to the parallel port data register. The CPU can also set or clear control bits AutoFeed (AFD/), initialize printer (INIT/)(the backslash indicating an active low signal) and select input (SLIN). The control bit AFD/ determines how the printer reacts to a carriage return. The control bit INIT/ which causes the printer to initialize. The SLIN bit brings the printer allows the CPU to bring the printer on and off-line for printer designed to allow that. Further details on Standard mode operation can be found in the IEEE 1284 specification mentioned previously.

Toggle of a input pin must cause the port expansion bus time slot to send at least one change of state. Thus, if an input pin toggles from a 1 - 0 - 1, and the 0 changes back to 1 before the 0 has been placed onto the port expansion bus, then the time slot assigned to that input pin on the port expansion bus must reflect at least one change of state. Thus, for a 0 - 1 - 0 toggle, the port expansion bus time slot for that bit must transfer a 1 at the next frame after the toggle and then a 0 in the subsequent frame. In other words, any changes on the input pins must be latched and the input pin cannot be latch a changed state again until read. The CPU can also read the status of Error, Paper Empty (PE), Busy/, ACK/, Select (SLCT). The assertion of ACK/ and Busy pulse must also cause the port expansion bus time slot to send at least 1 change of state.

PS2 mode provides a read enhancement to the Standard mode so that it becomes a Read/Write version of the Standard Mode. PS2 Mode The write operation is the same as Standard mode except that the CPU sets the Direction bit, which drives the PDIR pin, indicating the direction of transfer. The Read operation is the same as Write except that the Strobe signal is tri-state and busy is not used. Data is latched on the trailing edge of ACK/.

Figures 12a and 12b shows the bit assignments for data transmitted over the two dedicated date lines for Standard and PS2 mode operation for the parallel port. The bits are numbered with respect to the leading edge of frame sync. Unlike the assignments for the other ports controlled through Data In and Data Out, the field sent over Parallel Data In and Parallel Data Out line is repeated six times every frame. The content of each data field is the same and is described for field 0. The data field includes a valid bit indicating that data in the field is valid (bit 0), 8 bits of data (bits 2:9) to transmit to the printer port, a STB/, PDIR, INIT/, AFD/,SLIN (bits 10:14, respectively) and several reserved bits. The use of multiple time slots for the same function, i.e., repeating the data field six times per frame, reduces the latency of parallel port data transmitted over the port expansion bus. In a similar fashion, the parallel port frame received from the port expansion circuit has six data fields containing data received on the parallel port from the port expansion circuit. Each data field includes a valid bit indicating that data in the field is valid, 8 bits of data received from the printer port (bits 2:9), a Busy, ACK/, PE, SLCT, ERR/ (bits 10:14, respectively) and several reserved bits.

The Extended Capabilities Port (ECP) mode provides totally automated read and write cycles. It is FIFO-based and uses DMA. The FIFOs are in the South Bridge. There is a Run Length Encoding (RLE) compression option. The read expansion is done in hardware and the write compression done in software.

In ECP Mode, a typical Write operation of Command or Data to a printer works as follows. The CPU writes data to the Data Register in the South Bridge. Note that the data may be an address. Alternatively, the CPU may write to the FIFO in the South Bridge or DMA may be used. Port logic in the port expansion circuit generates Strobe/(pulse) automatically when a write takes place instead of requiring the CPU to write a control register as in Standard mode. The printer responds with Busy. The trailing edge of Busy allows Strobe/ to go inactive. The AFD/ pin, which is used as the Command/Data indication, is cleared or set according to the tag bit sent with each data byte (the FIFO contains one tag bit per byte).

The Direction pin (static) is controlled by software (a tag field is included with each data byte indicating direction).

- 10 An ECP Mode, Read operation, Non-Compressed, includes the following steps. The CPU sets the Direction bit to indicate input. Printer sends data which is latched into the port expansion circuit on the trailing edge of ACK/. The leading edge of ACK/, from peripheral causes the port expansion circuit state machine to activate AFD. The trailing edge of ACK/ allows the port expansion circuit to deactivate AFD.

- 15 Data is sent to the FIFO in the South Bridge via the port expansion bus. IRQ or DMA is generated by the South Bridge and the FIFO is read.

For ECP Mode, Read operation which is compressed the RLE expansion on data received over the parallel port takes place in the South Bridge. The Busy signal from the printer indicates the location of the RLE count byte. An RLE tag bit is sent with the data field back to the South Bridge (via the port expansion bus), indicating whether the data field contains an RLE count or Data.

- 20 Figures 13a and 13b show the bit assignments for data transmitted over the two dedicated data lines for ECP mode operations. The bits are numbered with respect to the leading edge of frame sync. Like the assignments for Standard/PS2 operating modes, the fields are repeated six times for each frame. The content of each data field is the same and is described for field 0. The data field includes a valid bit indicating that data in the field is valid (bit 0), a Data-CMD bit (bit 1), 8 bits of data/CMD (bits 2:9) to transmit to the printer port, INIT/AFD/, SLIN (bits 12:14, respectively) and several reserved bits. The use of multiple time slots for the same function, i.e., repeating the data field six times per frame, reduces the latency of parallel port data transmitted over the port expansion bus. In a similar fashion, the parallel port frame received from the port expansion circuit has six data fields containing data received on the parallel port from the port expansion circuit. Each data field includes a valid bit indicating that data in the field is valid, an RLE bit indicating if the byte is an RLE byte, 8 bits of data received from the printer port (bits 2:9), PE, SLCT, ERR/ (bits 12:14, respectively) and several reserved bits.
- 25
- 30

The Enhanced Parallel Port (EPP) mode provides partially automated Read and Write cycles, i.e., the CPU does a read or write and the parallel port builds the parallel port timing. The CPU cycle is extended via

IOCHRDY while the port cycle takes place. IOCHRDY is a signal that can be utilized by an expansion device on the ISA bus to cause wait states to be inserted in the bus cycle until the device is ready.

The EPP mode operates generally as follows. The AFD/ signal provides a Data strobe signal indicating that data is present on the data pins. The SLCTIN/ signal provides an Address strobe signal
5 indicating that an address is present on the data pins.

The Strobe/ pin provides a Write cycle indicator. When the pin is high, a high value on the pin indicates a read operation a low value indicates a write operation. The BUSY pin provides a Strobe from printer indicating that data is valid from the printer.

An EPP mode Write operation for an Address is as follows. The CPU sets the direction (write in this
10 case), which drives Strobe. The CPU writes data to the address port register. The leading edge of IOW/ (I/O Write Command on the ISA bus) drives SLCTIN/, and IOCHRDY back to the CPU which can also be delayed until the leading edge of Busy. The SLCTIN/ pin provides the address strobe indicating that address information is contained on the pins. The printer asserts Busy. The port expansion circuit parallel port control logic drops SLCTIN/ in response to busy. The port expansion circuit parallel port drops Strobe, data, and
15 IOCHRDY in response to Busy.

An EPP Write operation for data is the same as an "address" operation except the CPU writes to the Data register instead of the Address register. The SLCTIN/ pin is replaced by the AFD/ pin which provides the data strobe.

An EPP Read operation for an Address includes the following. The CPU write sets the direction
20 (read in this case), which drives Strobe. The CPU reads the Address register, driving SLCTIN/ and IOCHRDY/. The peripheral responds by driving data onto the parallel port and activating Busy. Busy going active causes data to be latched into the port expansion circuit, SLECTIN/ to be deactivated and IOCHRDY to be deactivated. Deactivation of IOCHRDY allows the CPU to end the read cycle

The parallel port logic in the South Bridge contains a timer that generates an 10µs error if the
25 peripheral does not respond (Busy signal).

An EPP Read operation for data is the same as for "address" except the CPU reads from the Data register instead of the Address register. The AFD/ pin which provides the data strobe is asserted instead of SLCTIN/.

Note that EPP mode operates quite differently from all other modes in that the parallel port bit time
30 slot assignments are not aligned with frame sync. The bit time slot assignments are shown in Figure 14a for an EPP write mode. Although EPP frames are not aligned to frame sync, the bit time slots are still synchronous to the bit clock. For an EPP mode write operation, an EPP frame starts with the receipt of a Start Bit. The bus (i.e., the dedicated parallel port data in and data out lines) zero-idles until a one is received,

which is a start bit. The first bit received after the Start Bit indicates whether the parallel port will write or read data. The next bit indicates whether the contents of the data pins will be address or data. For write operations, the next 8 bits are the data to be transmitted. At all other times the transmit side of the bus zero idles (from the South Bridge to the port expansion circuit). Following the receipt of the Start Bit, the receive side reflects the state of the Busy pin. The transition from 1 to 0 on the Busy pin indicates the end of the write transaction.

Figure 14b shows the bit assignments for an EPP Mode Read Operation. An EPP read cycle starts with the receipt of a valid Start Bit (from the South Bridge), followed by the Read-Write bit (set to 1) and the Address-Data bit. The parallel port logic within the ECP will then generate a read cycle. In the receive direction, the bus will zero-idle until the read data is received from the peripheral device connected to the bus. Upon receipt of the data, the port expansion circuit will send it to the South Bridge by first sending a start bit, followed by the 8 data bits.

Another port that does not use pin reflection for all functions is the game port. The game port has four reflected pins which are the status of joystick buttons (3:0) and four pairs of non-reflected pins. The four non-reflected pairs are used to transmit commands to the port expansion circuit to read the four joystick(s) X and Y positions and receive back the associated done indications.

Because of their analog nature, the game port comparators are preferably located in the port expansion circuit. User software writes to the Game Control Register (ISA legacy address 201h) requesting that the comparators measure the joystick position. The request is sent to the port expansion circuit via bits 65:68 as shown in Figure 8a. When the comparison(s) are complete, the corresponding done bit(s) are set. At the South Bridge side, the status bits in the Game Control Register are updated upon the transition of the respective done bits (bits 65:68) in the frame received from the port expansion circuit.

Referring to Figure 15, the game port supports connection of up to two joysticks 1501 and 1503 with a total of four buttons. The status of the buttons is provided over the GAMIN pins. Trim digital to analog converters (DACs) are provided to adjust the offset voltage for calibration. Each joystick contains a potentiometer for each of the X and Y directions and two buttons. Software uses the game port to determine the X and Y position of each of the joysticks and to determine the state of each of the buttons. The four GAMIN pins 1505 are internally pulled up through a 6K ohms (nominal; + or - 2K ohms) resistor in the port expansion circuit.

Traditionally, software uses the GAMIO pins to determine the joystick position. by (1) writing to the game port—setting the GAMIO pins to the high-impedance state—and (2) polling the game port continuously and using the count of the number of reads to determine when each of the GAMIO bits toggle to determine the time to charge the external capacitor through the X and Y potentiometers in the joystick.

Referring to Figure 16, an example of the operation of a single potentiometer 1601 indicating either the X or Y direction of joystick 1600. Logic 1610, which resides in the port expansion circuit includes a voltage source 1605, a comparator 1607, a flip-flop 1609 and a game control register 1611.

The external potentiometer 1601 in the joystick normally ranges from 2.2K to about 100K ohms.

- 5 The external capacitor 1613 is normally 5600 picofarads (pF). The high-impedance time for the pin can be calculated by the following formula:

$$\text{time} = -R C \ln(1 - (V_{th}/V_{cc}));$$

- Where V_{th} is the threshold voltage of 2.5 volts, V_{cc} is the pull-up voltage to the potentiometer 1601 (5.0 or 3.3 volts), R is the resistance of the potentiometer, and C is the capacitance of capacitor 1613. If V_{cc} is 5 volts, then the time will vary from about 8 to 388 microseconds. If V_{cc} is 3.3 volts, then the time will
10 vary from about 20 to 1000 microseconds.

- Figure 17 shows a charging diagram for the operation of the circuit shown in Figure 16. The four GAMIO pins can be in three possible states: ground, high-impedance, and transition-to-ground. The time the RC circuit takes to charge up to 2.5 volts is determined by sampling of the game port. Once the GAMIO voltage exceeds 2.5 volts, the comparator 1607 sends an indication to the GAMIO Control flip-flop 1609
15 which turns on transistor 1615 which causes the RC circuit to return to a ground state.

- No matter how much integration takes place, there seems to always be a need for some glue logic on the motherboard. Additionally, there is a need for a number of general-purpose I/O pins that can be accessed and controlled via software. It is advantageous to provide a number of I/O pins connected to programmable logic such as a Programmable Logic Array (PLA) internal to the port expansion circuit. These pins can be
20 used "locally" to perform some logic function that is not connected with the South Bridge (just like random logic on the motherboard), or it can be used in connection with the more traditional General I/O functions associated with SIO chips.

- Figure 18 illustrates one example. Suppose the motherboard has an LED that indicates whether a switch is open or closed, but only when the PC is in a particular mode of operation. This is a simple AND
25 function. When the PC state = true (as indicated by latch 1801) AND switch = true, then LED = ON, else LED = OFF. One signal (the switch) is an input to the PLA via one of the port expansion circuit's general I/O pins 1803. The other input comes from latch 1801 which is set by software. The latch is in the South Bridge, and reflected to the port expansion circuit over the bus using one of the General Purpose I/O time slots shown in Figure 8a as bits 84:95. The result of the AND operation is output on another of the port expansion
30 circuit's I/O pins 1807.

The PLA can be programmed via SRAM, Flash EPROM, or fuses. In the SRAM or EPROM embodiment, one of the commands in the link command field, (bits 1:8) may be used to indicate that the

following data in the frame is intended for the SRAM or EPROM. That data will include at least a starting address for the data destined for the SRAM or EPROM.

5 Other functions are also advantageously located on the port expansion circuit IC. PC motherboards require a number of clock signals. These are normally produced from a single crystal using a clock synthesizer IC (e.g., Cypress CY2254). It is advantageous to integrate the clock synthesis function into the port expansion circuit for the following reasons. The port expansion circuit is in a process that is well suited for this type of quasi-analog function. Further, greater control over power management is offered by putting the clock synthesis function in the chipset.

10 The port expansion circuit is pad-limited (meaning that the minimum size of the IC, as determined by the number of pins located around the outside edge of a square, is larger than the area necessary to contain the chip's logic). Thus, adding the function produces little marginal cost increase and integration reduces motherboard chip count, board space, and cost.

The clock synthesizer is controlled via messages sent over the Command channel. Status is returned via the response channel. The start-up state of the clock synthesizer is selected via option selection pins.

15 Other functions are also controllable. All of the pins associated with the floppy disk controller can be remoted. The read and write data pins can only be remoted if the data separation function is located in the port expansion circuit, otherwise, separate dedicated pins are required on the South Bridge.

20 Power management is becoming more and more of an issue as PCs are being designed to be powered on all of the time. The PC is adopting modes of operation similar to those of VCRs where the powered is always on, but the VCR is often "sleeping." The South Bridge, and thus the port expansion circuit, play an active role in power management. Two types of power management function must be covered: 1) placing the internal logic and I/O pins in one of several correct states depending on the power mode of the PC; and 2) controlling the operating state of the rest of the system. The first case is simply a matter of communicating the desired power mode to the port expansion circuit via the port expansion bus Command channel.

25 The second case involves the relationship of the various I/O functions (especially the General Purpose I/O pins) and the functional blocks within the South Bridge. For example, activity on the control pins of a COM port, say the Ring Indicate pin, must wake up the PC from sleep mode. A way must be provided for the port expansion circuit to request that the South Bridge start up the bus clocks (Bit Clock and Frame Sync). (These clocks are stopped when the PC enters sleep state to reduce power consumption.)

30 Referring to Figure 1901, when the bus is stopped to reduce power consumption as shown at region 1901, all of the lines on the port expansion bus are kept high. The port expansion circuit can request that the bus be restarted by pulling the Data In pin low 1903 (Data In is an output from the port expansion circuit to the South Bridge). The Data In pin should be held low until frame sync goes low. Frame sync must go low

for at least one bit time 1907 before it can go high (signifying the start of a frame). Note that while the protocol for waking up have been described with respect to specific polarities, other polarities can also be used depending upon the choice for indicating assertion of a signal.

5 The desired power mode can be one of several. For instance, there may be five separate power management states. The first is an on state in which normal power up state exists. The second state is a power off state. A third state is a sleep state in which activity on one of the ports can wake up the port expansion circuit but the clocks are stopped and there is very low power consumption. In a fourth state the port expansion circuit is in a sleep state with power being supplied at some level but can not wake up the host (the South Bridge) on account of activity on port expansion circuit ports. The port expansion circuit can only wake
10 up when the host instructs the port expansion circuit to wake up. In a fifth state, portions of the port expansion circuit, e.g., particular ports are selectively on.

 The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For instance, the invention has been described with the expansion bus being the ISA bus. In other embodiments, the expansion bus may be different. For instance, as
15 PC architecture continues to evolve, the PCI bus may become the input/output bus that is presently the ISA bus in the embodiment described above and the legacy devices may be those that interface to the PCI bus today. In such an embodiment, the South Bridge would provide an interface between PCI legacy devices and the PCI bus. Other buses may also serve as the input/output or expansion bus such as the MCA bus. Variations and modifications of the embodiments disclosed herein, may be made based on the description set
20 forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.

WHAT IS CLAIMED IS:

- 1 1. An apparatus comprising:
2 a first integrated circuit including a functional circuit;
3 a second integrated circuit providing input and output terminals for the functional circuit; and,
4 a bus coupling the first and second integrated circuits, the bus transferring data substantially
5 continuously between the first and second integrated circuits, the data including output
6 signals from the functional circuit provided to the output terminals of the second integrated
7 circuit and input signals for the functional circuit from the input terminals of the second
8 integrated circuit.
- 1 2. The apparatus of claim 1 wherein the data is transferred between the first and second
2 integrated circuits in frames, each frame including a predetermined number of data bits, each frame including
3 predetermined slots for the states of the input and output signals, so as to continuously transfer the state of the
4 input and output signals to and from the input and output pins of the second integrated circuit at a
5 predetermined rate.
- 1 3. The apparatus as recited in claims 1 or 2, wherein the functional circuit includes:
2 an input/output bus;
3 a plurality of interfaces coupled to the input/output bus, the interfaces providing an interface between
4 the input/output bus and a plurality of devices.
- 1 4. The apparatus of claim 3 wherein the input/output bus conforms to an industry standard
2 architecture (ISA) and the plurality of interfaces are ISA interfaces.
- 1 5. The apparatus as recited in claim 4 wherein the second integrated circuit includes
2 input/output terminals to couple to at least one legacy device.
- 1 6. The apparatus as recited in claim 5 wherein the plurality of ISA interfaces in the first
2 integrated circuit include an interface for at least one legacy device.
- 1 7. The apparatus as recited in claim 6 wherein the at least one legacy device is one of a serial
2 port and a keyboard and a mouse and a game port and a MIDI port and a floppy drive and a PC speaker and at
3 interface for the at least one legacy device connects to the at least one legacy device through the input/output
4 terminals of the second integrated circuit.
- 1 8. The apparatus of claim 1, wherein the first integrated circuit operates at a lower voltage than
2 the second integrated circuit.

1 9. The apparatus of claim 1, wherein the first integrated circuit is comprised of a majority of
2 transistors whose channel lengths are at least as small as a first value and wherein the second integrated circuit
3 is comprised of transistors all of whose channel lengths are longer than the first value.

1 10. The apparatus as recited in claim 1, further comprising:
2 a processor;
3 a bridge integrated circuit coupled to the processor;
4 a PCI bus coupled to the bridge integrated circuit and the first integrated circuit.

1 11. A method of partitioning input/output functions between a first and a second integrated
2 circuit, the first integrated circuit including a plurality of logic interfaces between an input/output bus and
3 respective external devices, comprising the steps of:
4 generating a plurality output signal values in the plurality of logic interfaces for the external devices;
5 transmitting the plurality of output signal values from the first integrated circuit to the second
6 integrated circuit over a substantially continuously operating bus;
7 providing the output signal values to output terminals of the second integrated circuit;
8 receiving input signal values from the external devices onto the second integrated circuit; and
9 transmitting the input signal values from the second to the first integrated circuit over the bus.

1 12. The method as recited in claim 11 wherein the input/output bus conforms to an industry
2 standard architecture bus.

1 13. The method as recited in claim 11 wherein the external devices are PC legacy devices.

1 14. The method as recited in claim 13 wherein the PC legacy devices include at least one of a
2 keyboard and a mouse and a game port and a MIDI port and a floppy drive and a PC speaker and a device
3 connected through a serial port.

1 15. The method as recited in claim 11 wherein the transmitting takes place over a serial bus.

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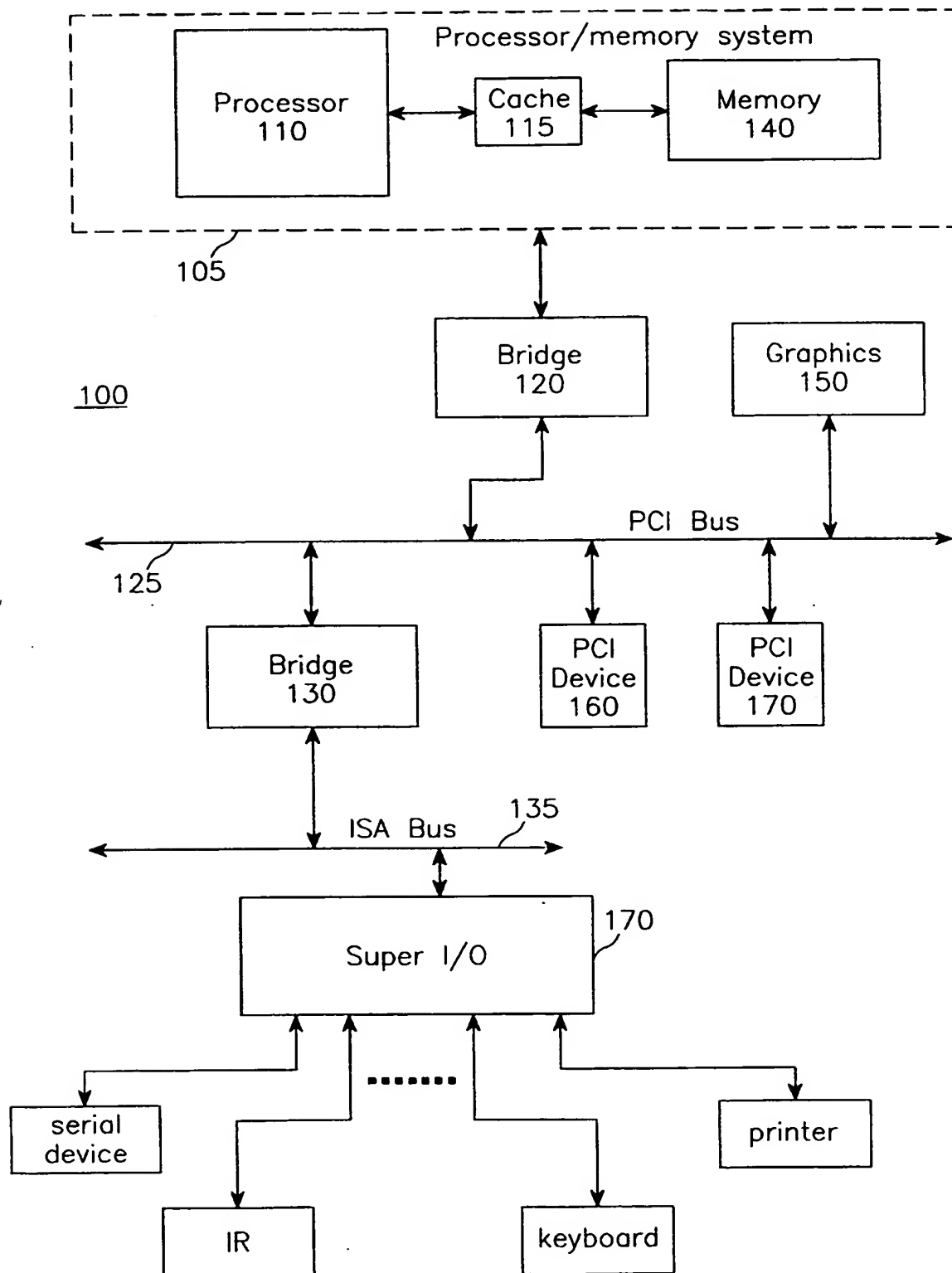


FIG. 1

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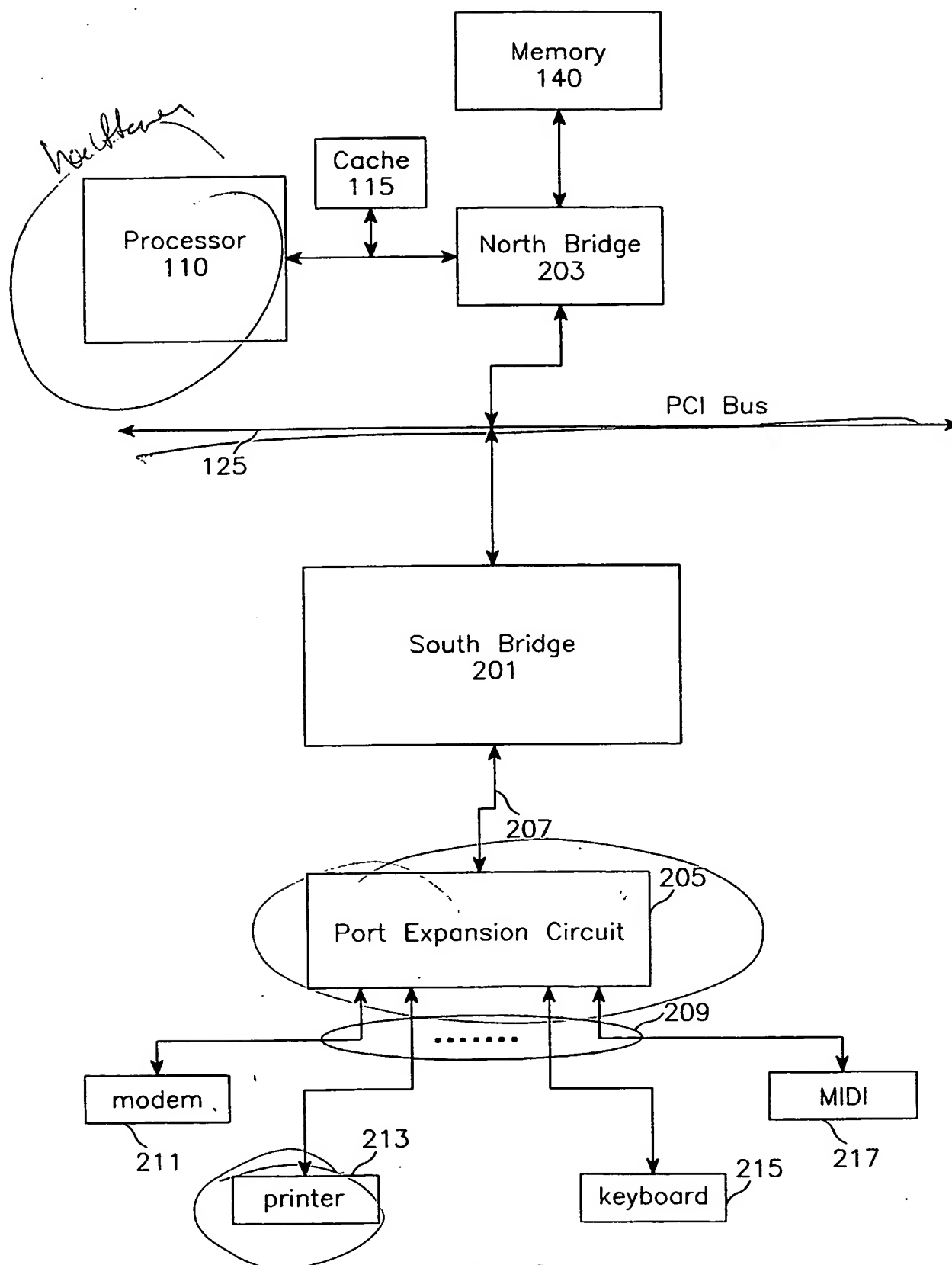


FIG. 2

3/20

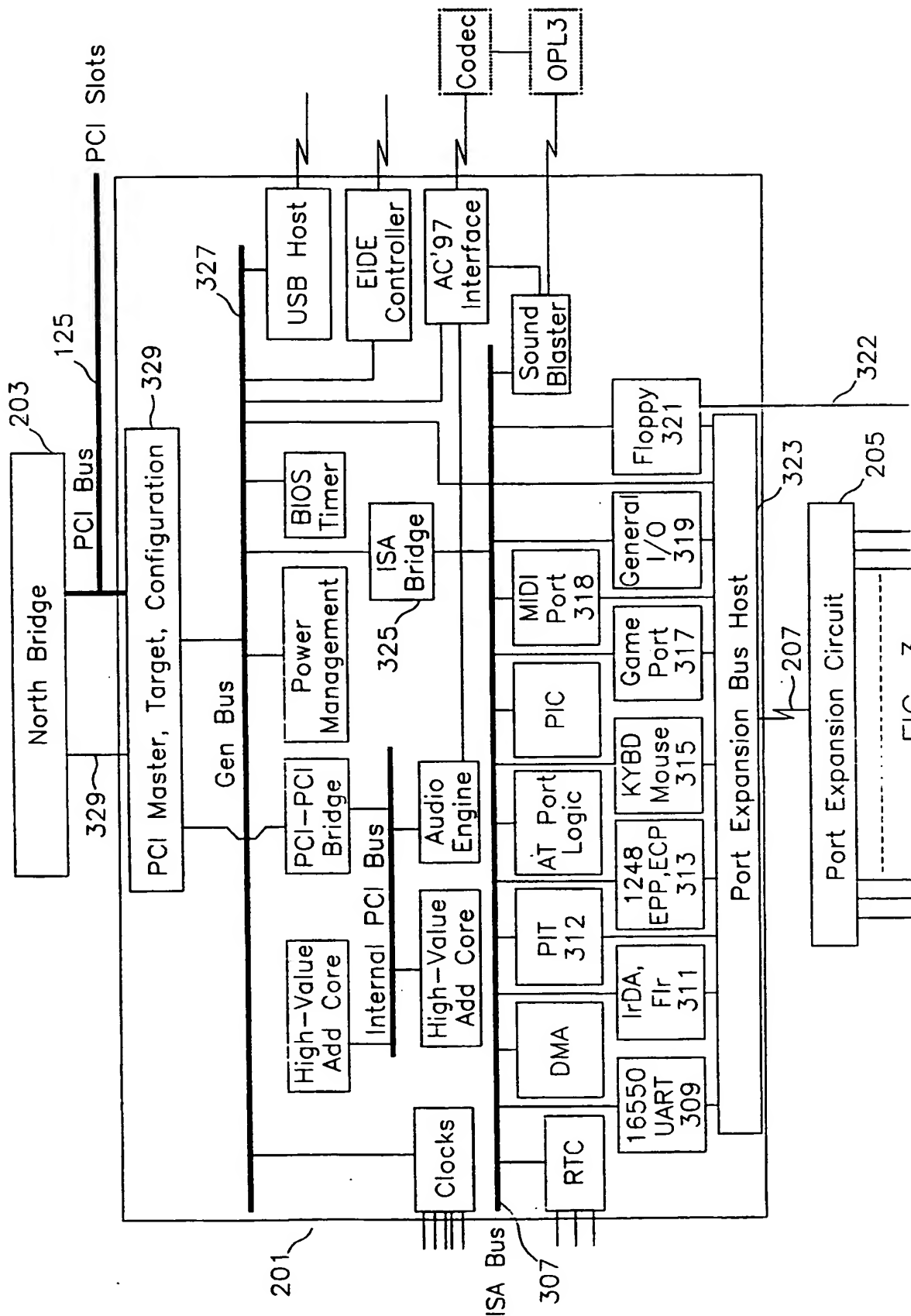


FIG. 3

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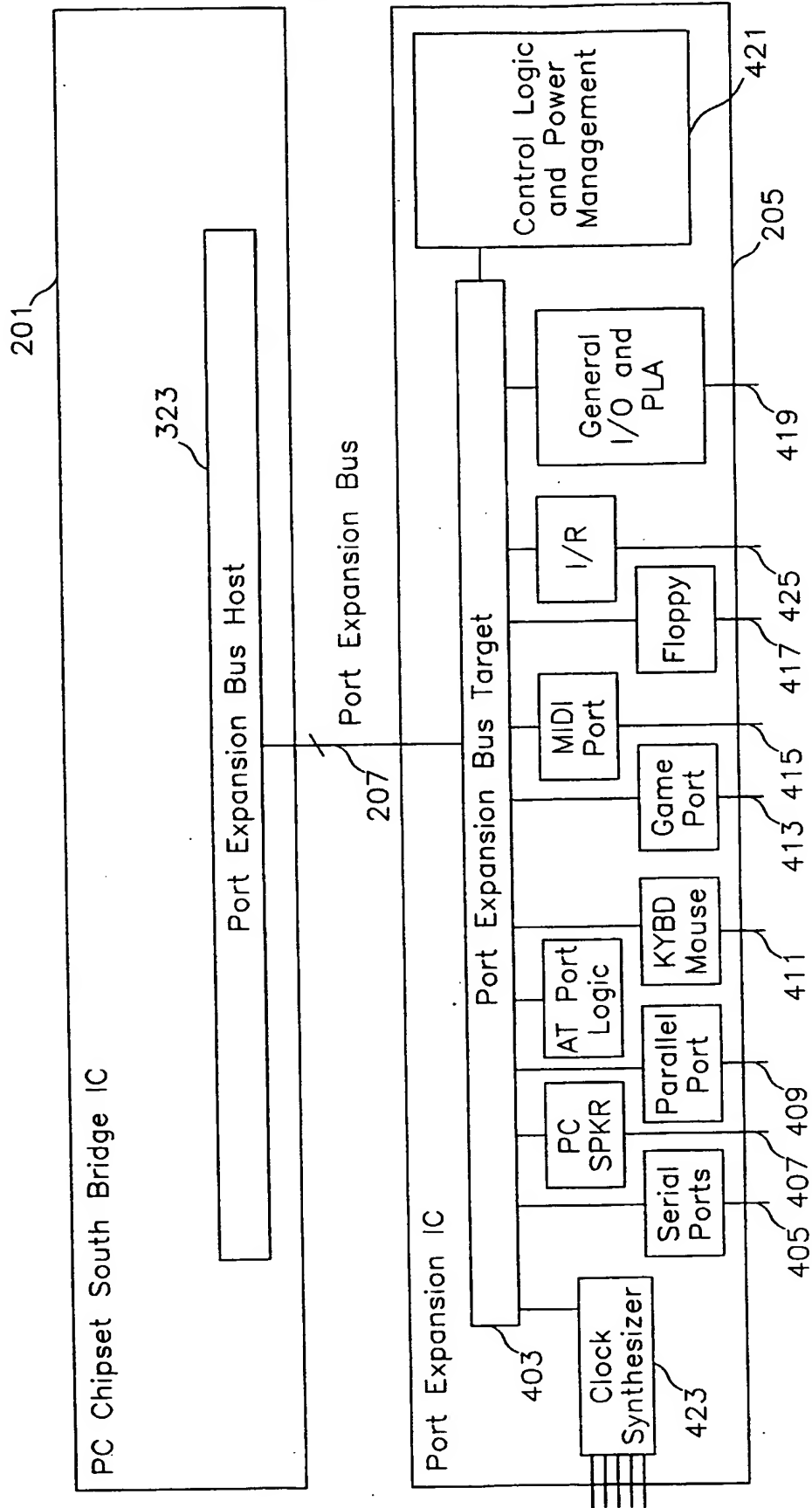


FIG. 4

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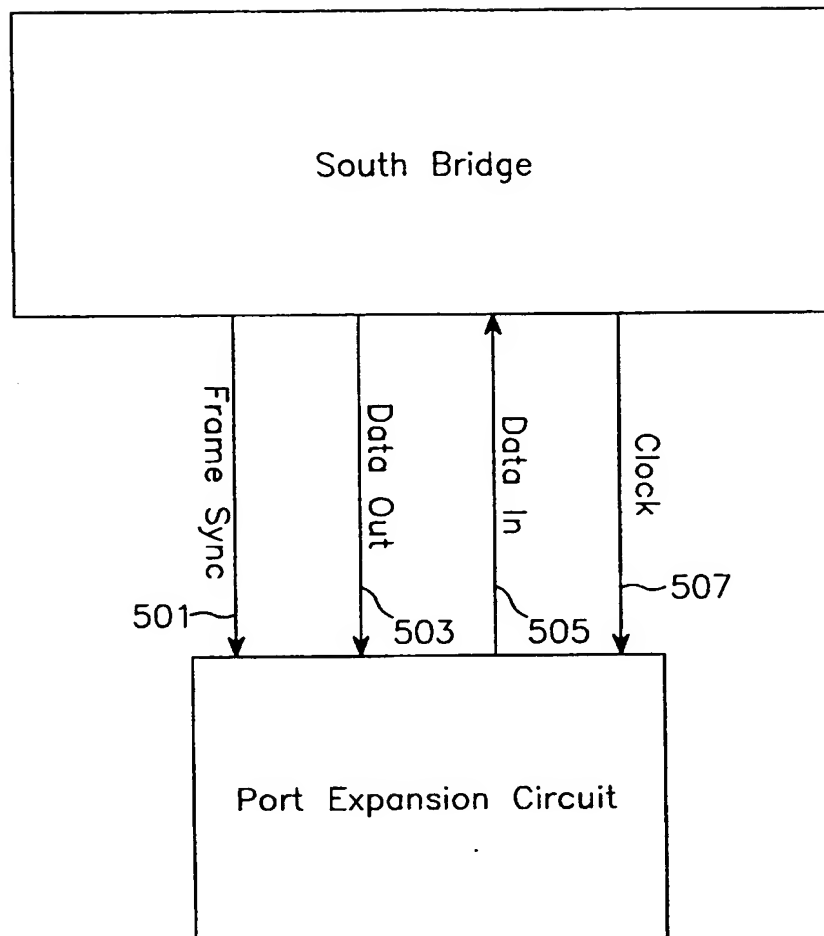


FIG. 5

6/20

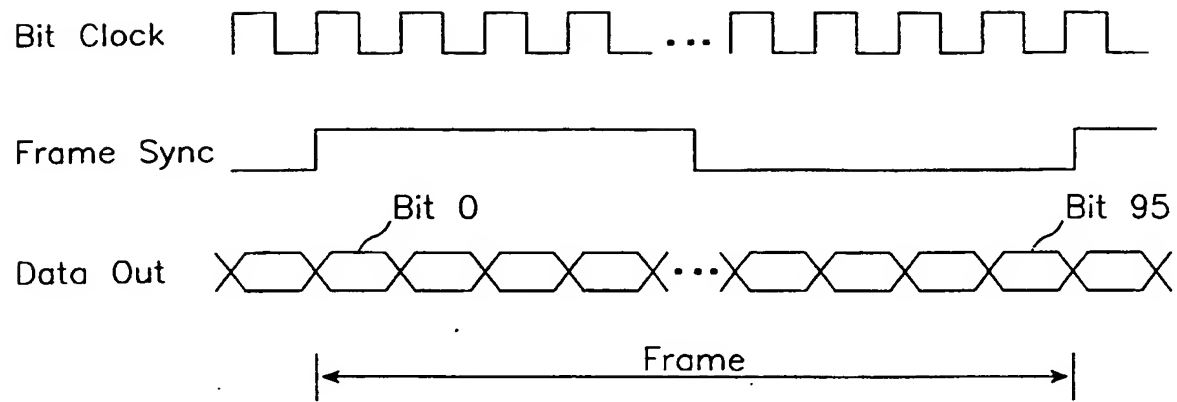


FIG. 6

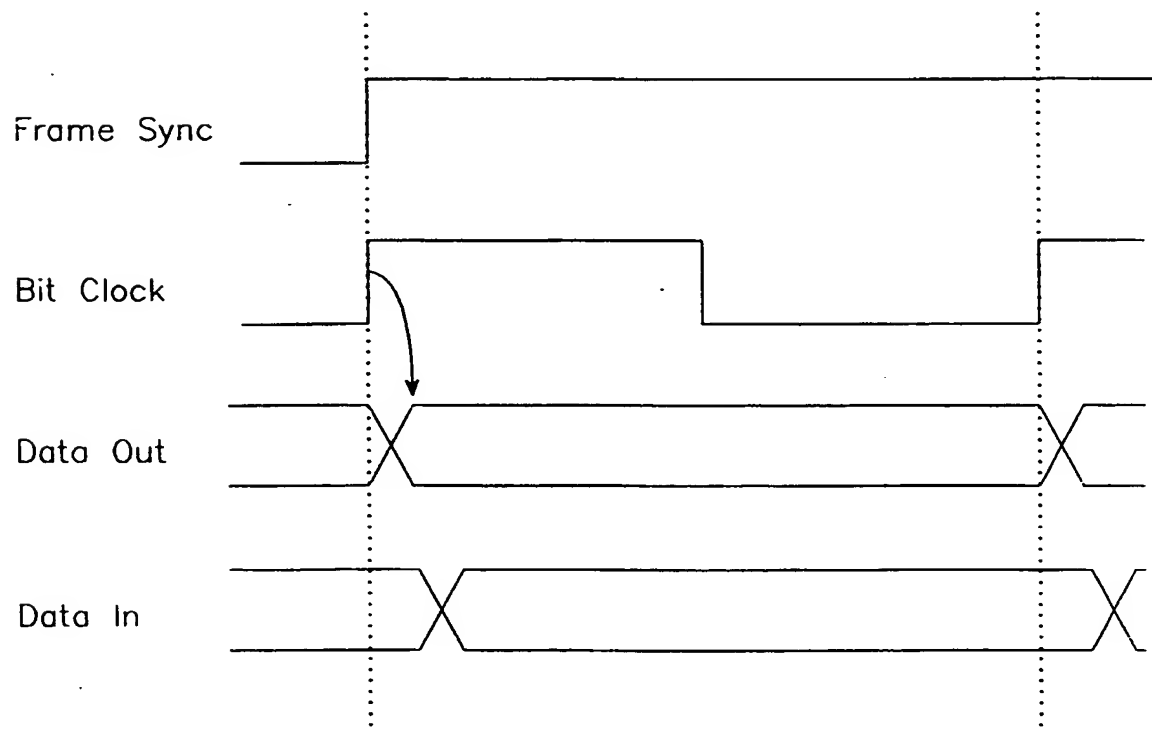


FIG. 7

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Bit#	Function
0	Command Valid
1	Link command bit 0
2	bit 1
3	bit 2
4	bit 3
5	bit 4
6	bit 5
7	bit 6
8	Link command bit 7
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved
32	Floppy WGATE/
33	Floppy HDSEL/
34	Floppy DIR/
35	Floppy STEP/
36	Floppy MTR0/
37	Floppy MTR1/
38	Floppy DR0/
39	Floppy DR1/
40	Floppy DENSEL
41	Floppy DRATE0
42	Floppy DRATE1
43	Reserved
44	Reserved
45	Reserved
46	Reserved
47	Reserved

Bit#	Function
48	Serial port 0 RTS/
49	Serial port 0 DTR/
50	Serial port TD
51	Reserved
52	Reserved
53	Serial port 1 RTS/ (or kybd tx)
54	Serial port 1 DTR/ (or IrDA or mouse)
55	Serial port 1 TD (or IrDA or mouse)
56	Reserved (or IrDA or mouse)
57	Reserved (or IrDA or mouse)
58	Reserved
59	Reserved
60	Reserved
61	Reserved
62	Reserved
63	Reserved
64	Reserved
65	Game X0 request
66	Game X1 request
67	Game Y0 request
68	Game Y1 request
69	Reserved
70	Reserved
71	Reserved
72	Reserved
73	Reserved
74	Reserved
75	Reserved
76	Reserved
77	Reserved
78	Reserved
79	Reserved
80	Reserved
81	Reserved
82	PC speaker out
83	MIDI TX
84	User interface out
85	User interface out
86	User interface out
87	User interface out
88	User interface out
89	User interface out
90	User interface out
91	User interface out
92	User interface out
93	User interface out
94	User interface out
95	User interface out

FIG. 8A

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Bit#	Function
0	Response/status
1	Link status bit 0
2	bit 1
3	bit 2
4	bit 3
5	bit 4
6	bit 5
7	bit 6
8	Link status bit 7
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved
32	Floppy TRK0/
33	Floppy INDEX/
34	Floppy DSKCHG/
35	Floppy WP/
36	Reserved
37	Reserved
38	Reserved
39	Reserved
40	Reserved
41	Reserved
42	Reserved
43	Reserved
44	Reserved
45	Reserved
46	Reserved
47	Reserved

Bit#	Function
48	Serial port 0 CTS/
49	Serial port 0 DSR/
50	Serial port 0 DCD/
51	Serial port 0 RI
52	Serial port 0 RD
53	Serial port 1 CTS/(or kybd rx)
54	Serial port 1 DSR/(or IrDA or mouse)
55	Serial port 1 DCD/(or IrDA or mouse)
56	Serial port 1 RI (or IrDA or mouse)
57	Serial port 1 RD (or IrDA or mouse)
58	Reserved
59	Reserved
60	Reserved
61	Reserved
62	Reserved
63	Reserved
64	Reserved
65	Game X0 done
66	Game X1 done
67	Game Y0 done
68	Game Y1 done
69	Button 0
70	Button 1
71	Button 2
72	Button 3
73	Reserved
74	Reserved
75	Reserved
76	Reserved
77	Reserved
78	Reserved
79	Reserved
80	Reserved
81	Reserved
82	Reserved
83	MIDI RX
84	Vol +
85	Vol -
86	Mute
87	Keylock
88	Turbo
89	Setup disable
90	CLR CMOS
91	Sw 0
92	SW1
93	SW2
94	SW3
95	User interface in

FIG. 8B

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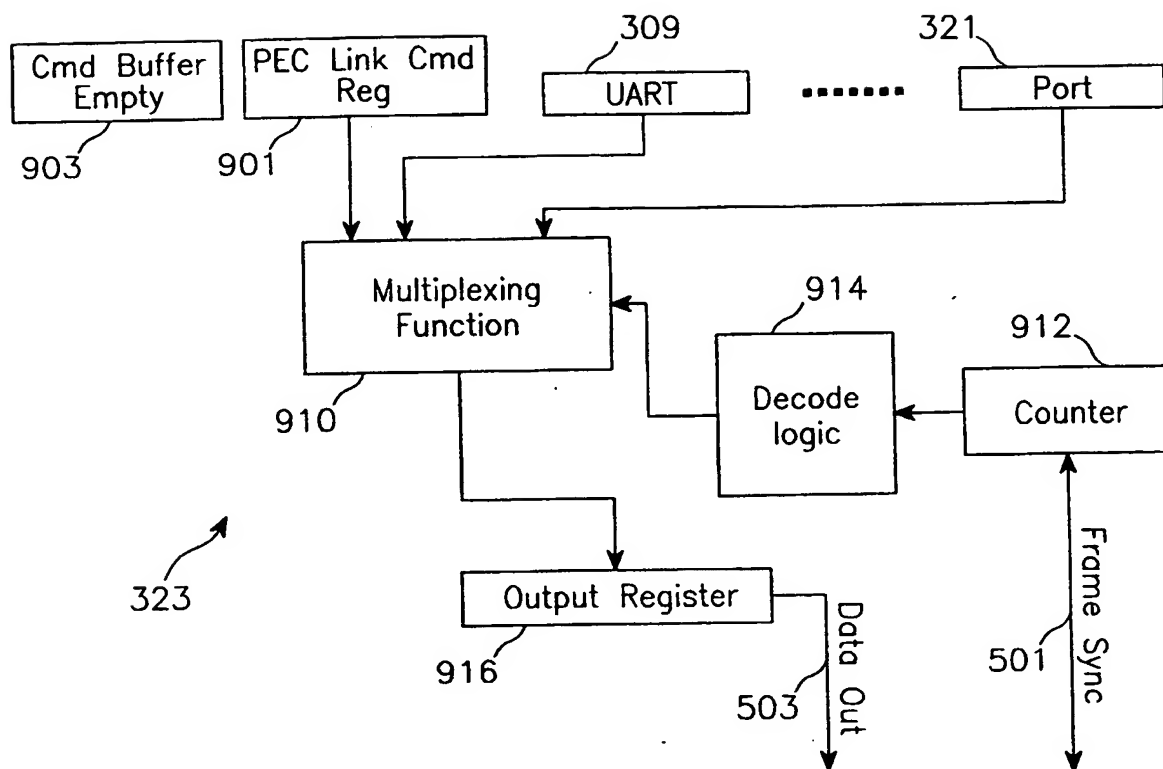


FIG. 9A

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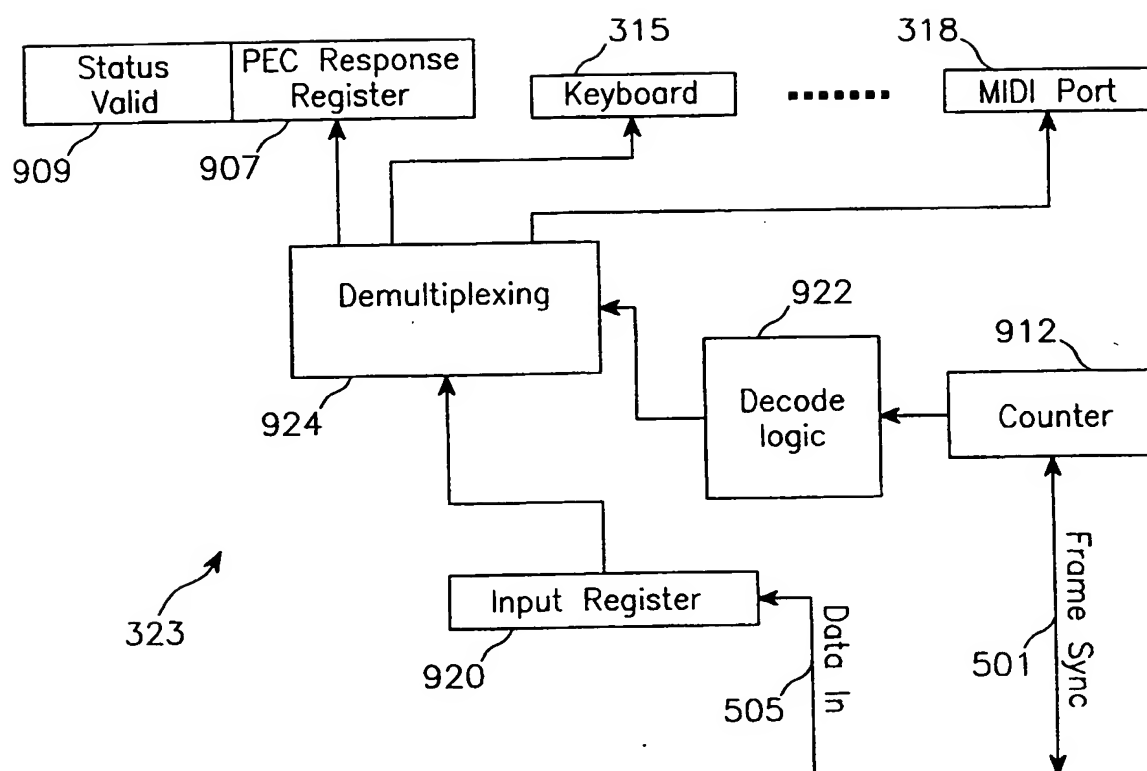


FIG. 9B

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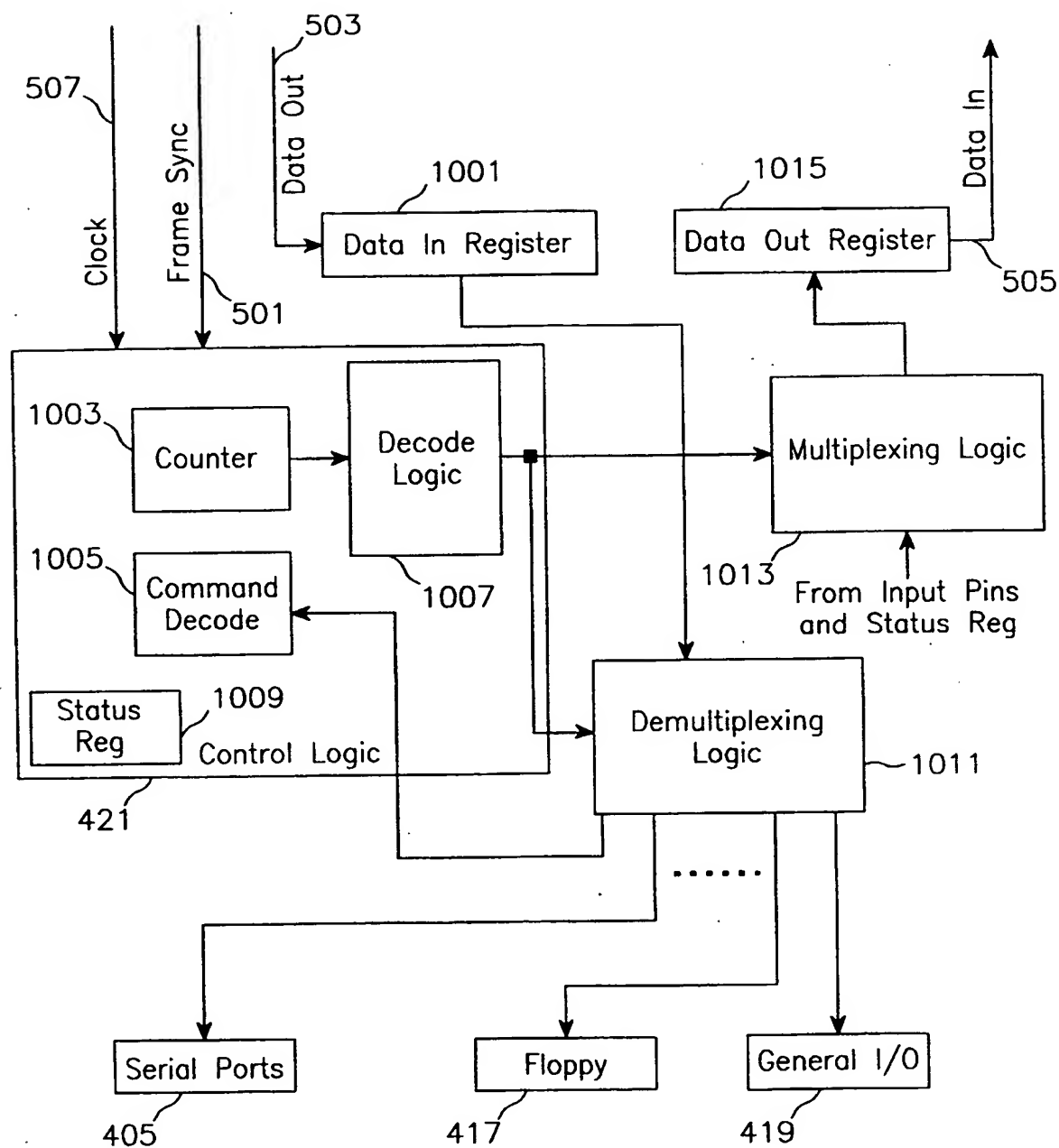


FIG. 10

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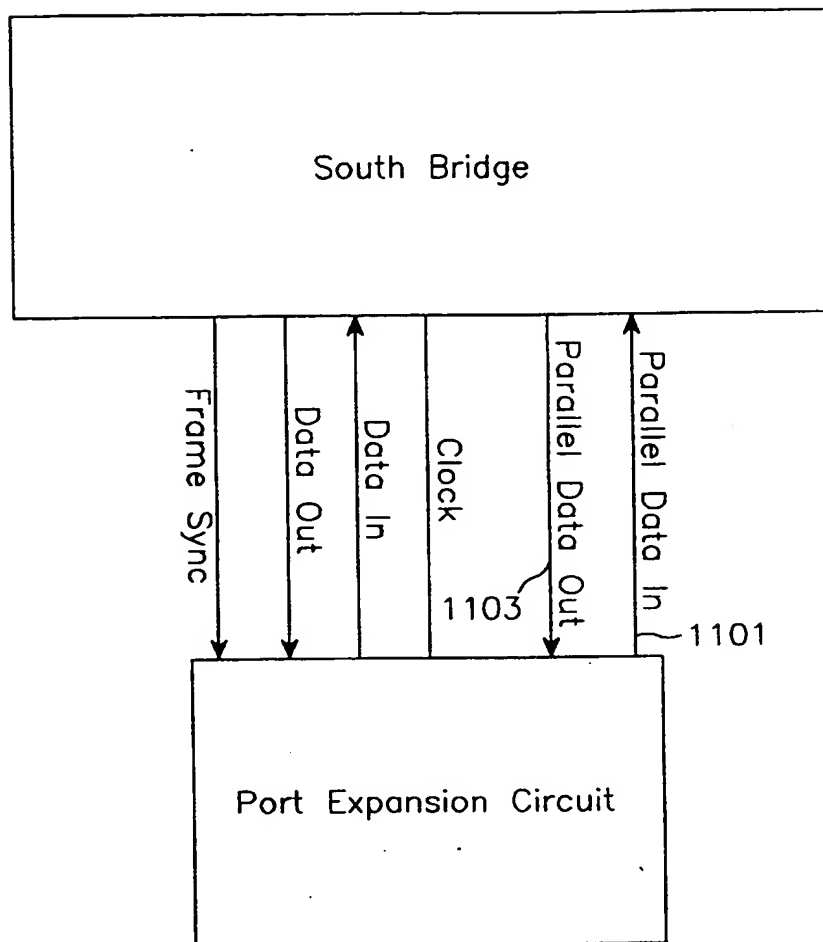


FIG. 11

Standard/ PS2 Mode Bit Assignments

Bit#	Function
0	Printer port data field 0 valid bit
1	Reserved
2	Printer port TX data field 0 bit 0
3	bit 1
4	bit 2
5	bit 3
6	bit 4
7	bit 5
8	bit 6
9	Printer port data field 0 bit 7
10	Printer port STB/
11	Printer port PDIR
12	Printer port INIT/
13	Printer port AFD/
14	Printer port SLIN/
15	Reserved
16	Printer port data field 1 valid bit
17	Reserved
18	Printer port TX data field 1 bit 0
19	bit 1
20	bit 2
21	bit 3
22	bit 4
23	bit 5
24	bit 6
25	Printer port data field 1 bit 7
26	Printer port STB/
27	Printer port PDIR
28	Printer port INIT/
29	Printer port AFD/
30	Printer port SLIN/
31	Reserved
32	Printer port data field 2 valid bit
33	Reserved
34	Printer port TX data field 2 bit 0
35	bit 1
36	bit 2
37	bit 3
38	bit 4
39	bit 5
40	bit 6
41	Printer port data field 2 bit 7
42	Printer port STB/
43	Printer port PDIR
44	Printer port INIT/
45	Printer port AFD/
46	Printer port SLIN/
47	Reserved

Bit#	Function
48	Printer port data field 3 valid bit
49	Reserved
50	Printer port TX data field 3 bit 0
51	bit 1
52	bit 2
53	bit 3
54	bit 4
55	bit 5
56	bit 6
57	Printer port data field 3 bit 7
58	Printer port STB/
59	Printer port PDIR
60	Printer port INIT/
61	Printer port AFD/
62	Printer port SLIN/
63	Reserved
64	Printer port data field 4 valid bit
65	Reserved
66	Printer port TX data field 4 bit 0
67	bit 1
68	bit 2
69	bit 3
70	bit 4
71	bit 5
72	bit 6
73	Printer port data field 4 bit 7
74	Printer port STB/
75	Printer port PDIR
76	Printer port INIT/
77	Printer port AFD/
78	Printer port SLIN/
79	Reserved
80	Printer port data field 5 valid bit
81	Reserved
82	Printer port TX data field 5 bit 0
83	bit 1
84	bit 2
85	bit 3
86	bit 4
87	bit 5
88	bit 6
89	Printer port data field 5 bit 7
90	Printer port STB/
91	Printer port PDIR
92	Printer port INIT/
93	Printer port AFD/
94	Printer port SLIN/
95	Reserved

FIG. 12A

Standard/ PS2 Mode Bit Assignments

TRANSMIT FROM PEC		TRANSMIT FROM PEC	
Bit#	Function	Bit#	Function
0	Printer port data field 0 valid bit	48	Printer port data field 3 valid bit
1	Reserved	49	Reserved
2	Printer port RX data field 0 bit 0	50	Printer port RX data field 3 bit 0
3	bit 1	51	bit 1
4	bit 2	52	bit 2
5	bit 3	53	bit 3
6	bit 4	54	bit 4
7	bit 5	55	bit 5
8	bit 6	56	bit 6
9	Printer port data field 0 bit 7	57	Printer port data field 3 bit 7
10	Printer port Busy	58	Printer port Busy
11	Printer port ACK/	59	Printer port ACK/
12	Printer port PE	60	Printer port PE
13	Printer port SLCT	61	Printer port SLCT
14	Printer port ERR/	62	Printer port ERR/
15	Reserved	63	Reserved
16	Printer port data field 1 valid bit	64	Printer port data field 4 valid bit
17	Reserved	65	Reserved
18	Printer port RX data field 1 bit 0	66	Printer port RX data field 4 bit 0
19	bit 1	67	bit 1
20	bit 2	68	bit 2
21	bit 3	69	bit 3
22	bit 4	70	bit 4
23	bit 5	71	bit 5
24	bit 6	72	bit 6
25	Printer port data field 1 bit 7	73	Printer port data field 4 bit 7
26	Printer port Busy	74	Printer port Busy
27	Printer port ACK/	75	Printer port ACK/
28	Printer port PE	76	Printer port PE
29	Printer port SLCT	77	Printer port SLCT
30	Printer port ERR/	78	Printer port ERR/
31	Reserved	79	Reserved
32	Printer port data field 2 valid bit	80	Printer port data field 5 valid bit
33	Reserved	81	Reserved
34	Printer port RX data field 2 bit 0	82	Printer port RX data field 5 bit 0
35	bit 1	83	bit 1
36	bit 2	84	bit 2
37	bit 3	85	bit 3
38	bit 4	86	bit 4
39	bit 5	87	bit 5
40	bit 6	88	bit 6
41	Printer port data field 2 bit 7	89	Printer port data field 5 bit 7
42	Printer port Busy	90	Printer port Busy
43	Printer port ACK/	91	Printer port ACK/
44	Printer port PE	92	Printer port PE
45	Printer port SLCT	93	Printer port SLCT
46	Printer port ERR/	94	Printer port ERR/
47	Reserved	95	Reserved

FIG. 12B

ECP mode bit assignments

TRANSMIT TO PEC		TRANSMIT TO PEC	
Bit#	Function	Bit#	Function
0	Printer port data field 0 valid bit	48	Printer port data field 3 valid bit
1	Printer port data field 0 Data-CMD bit	49	Printer port data field 3 Data-CMD bit
2	Printer port TX data field 0 bit 0	50	Printer port TX data field 3 bit 0
3	bit 1	51	bit 1
4	bit 2	52	bit 2
5	bit 3	53	bit 3
6	bit 4	54	bit 4
7	bit 5	55	bit 5
8	bit 6	56	bit 6
9	Printer port data field 0 bit 7	57	Printer port data field 3 bit 7
10	Reserved	58	Reserved
11	Reserved	59	Reserved
12	Printer port INIT/	60	Printer port INIT/
13	Printer port AFD/	61	Printer port AFD/
14	Printer port SLIN/	62	Printer port SLIN/
15	Reserved	63	Reserved
16	Printer port data field 1 valid bit	64	Printer port data field 4 valid bit
17	Printer port data field 1 Data-CMD bit	65	Printer port data field 4 Data-CMD bit
18	Printer port TX data field 1 bit 0	66	Printer port TX data field 4 bit 0
19	bit 1	67	bit 1
20	bit 2	68	bit 2
21	bit 3	69	bit 3
22	bit 4	70	bit 4
23	bit 5	71	bit 5
24	bit 6	72	bit 6
25	Printer port data field 1 bit 7	73	Printer port data field 4 bit 7
26	Reserved	74	Reserved
27	Reserved	75	Reserved
28	Printer port INIT/	76	Printer port INIT/
29	Printer port AFD/	77	Printer port AFD/
30	Printer port SLIN/	78	Printer port SLIN/
31	Reserved	79	Reserved
32	Printer port data field 2 valid bit	80	Printer port data field 5 valid bit
33	Printer port data field 2 Data-CMD bit	81	Printer port data field 5 Data-CMD bit
34	Printer port TX data field 2 bit 0	82	Printer port TX data field 5 bit 0
35	bit 1	83	bit 1
36	bit 2	84	bit 2
37	bit 3	85	bit 3
38	bit 4	86	bit 4
39	bit 5	87	bit 5
40	bit 6	88	bit 6
41	Printer port data field 2 bit 7	89	Printer port data field 5 bit 7
42	Printer port STB/	90	Reserved
43	Printer port PDIR	91	Reserved
44	Printer port INIT/	92	Printer port INIT/
45	Printer port AFD/	93	Printer port AFD/
46	Printer port SLIN/	94	Printer port SLIN/
47	Reserved	95	Reserved

FIG. 13A

ECP mode bit assignments

RECEIVE FROM PEC		RECEIVE FROM PEC	
Bit#	Function	Bit#	Function
0	Printer port data field 0 valid bit	48	Printer port data field 3 valid bit
1	Printer port data field 0 RLE bit	49	Printer port data field 3 RLE bit
2	Printer port RX data field 0 bit 0	50	Printer port RX data field 3 bit 0
3	bit 1	51	bit 1
4	bit 2	52	bit 2
5	bit 3	53	bit 3
6	bit 4	54	bit 4
7	bit 5	55	bit 5
8	bit 6	56	bit 6
9	Printer port data field 0 bit 7	57	Printer port data field 3 bit 7
10	Reserved	58	Reserved
11	Reserved	59	Reserved
12	Printer port PE	60	Printer port PE
13	Printer port SLCT	61	Printer port SLCT
14	Printer port ERR/	62	Printer port ERR/
15	Reserved	63	Reserved
16	Printer port data field 1 valid bit	64	Printer port data field 4 valid bit
17	Printer port data field 1 RLE bit	65	Printer port data field 4 RLE bit
18	Printer port RX data field 1 bit 0	66	Printer port RX data field 4 bit 0
19	bit 1	67	bit 1
20	bit 2	68	bit 2
21	bit 3	69	bit 3
22	bit 4	70	bit 4
23	bit 5	71	bit 5
24	bit 6	72	bit 6
25	Printer port data field 1 bit 7	73	Printer port data field 4 bit 7
26	Reserved	74	Reserved
27	Reserved	75	Reserved
28	Printer port PE	76	Printer port PE
29	Printer port SLCT	77	Printer port SLCT
30	Printer port ERR/	78	Printer port ERR/
31	Reserved	79	Reserved
32	Printer port data field 2 valid bit	80	Printer port data field 5 valid bit
33	Printer port data field 2 RLE bit	81	Printer port data field 5 RLE bit
34	Printer port RX data field 2 bit 0	82	Printer port RX data field 5 bit 0
35	bit 1	83	bit 1
36	bit 2	84	bit 2
37	bit 3	85	bit 3
38	bit 4	86	bit 4
39	bit 5	87	bit 5
40	bit 6	88	bit 6
41	Printer port data field 2 bit 7	89	Printer port data field 5 bit 7
42	Printer port Busy	90	Reserved
43	Printer port ACK/	91	Reserved
44	Printer port PE	92	Printer port PE
45	Printer port SLCT	93	Printer port SLCT
46	Printer port ERR/	94	Printer port ERR/
47	Reserved	95	Reserved

FIG. 13B

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EPP WRITE mode bit assignments

TRANSMIT TO PEC		RECEIVE FROM PEC	
Bit#	Function	Bit#	Function
0	Start-Bit (=1)	0	0
1	Read-Write bit (0=write, 1=read)	1	Busy pin state
2	Address-Data bit (0=data,1=address)	2	Busy pin state
3	Printer port TX data bit 0	3	Busy pin state
4	bit 1	4	Busy pin state
5	bit 2	5	Busy pin state
6	bit 3	6	Busy pin state
7	bit 4	7	Busy pin state
8	bit 5	8	Busy pin state
9	bit 6	9	Busy pin state
10	Printer port TX data bit 7	10	Busy pin state
11	0	11	Busy pin state
12	0	12	Busy pin state
13	0	13	Busy pin state
14	0	14	Busy pin state
15	0	15	Busy pin state
.
N	0	N	Busy pin state Low

FIG. 14A

EPP READ mode bit assignments

TRANSMIT TO PEC		RECEIVE FROM PEC	
Bit#	Function	Bit#	Function
0	Start-Bit (=1)	0	0
1	Read-Write bit (0=write, 1=read)	1	0
2	Address-Data bit (0=data,1=address)	2	0
3	0	3	0
.
N	0	N	Start Bit (1)
N+1	0	N+1	Printer port RX data bit 0
N+2	0	N+2	bit 1
N+3	0	N+3	bit 2
N+4	0	N+4	bit 3
N+5	0	N+5	bit 4
N+6	0	N+6	bit 5
N+7	0	N+7	bit 6
N+8	0	N+8	Printer port RX data bit 7

FIG. 14B

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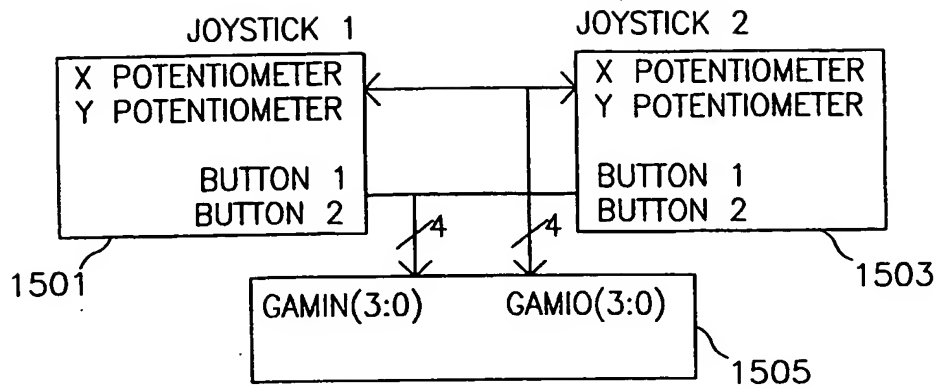


FIG. 15

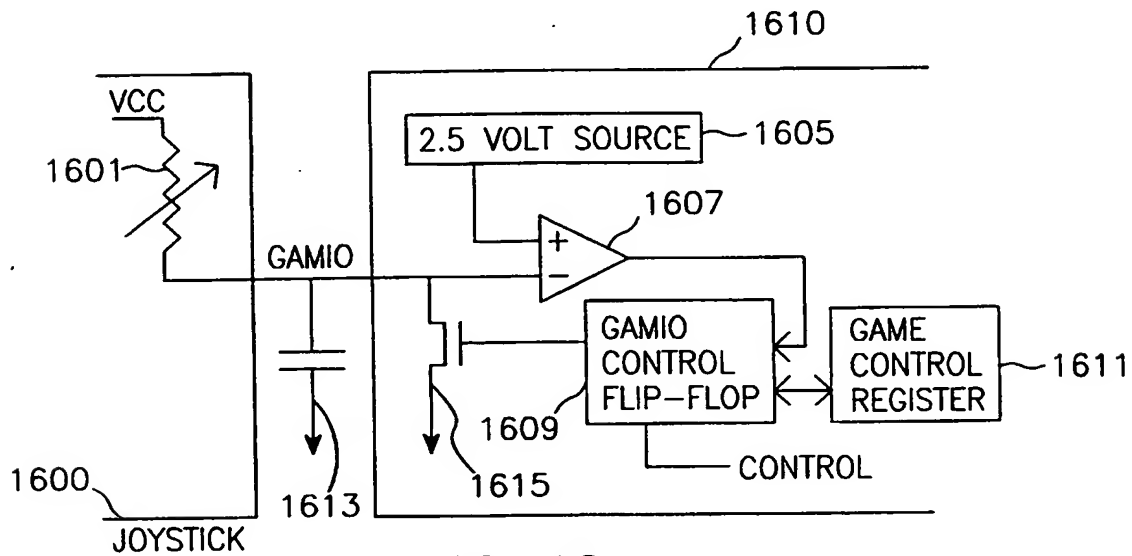


FIG. 16

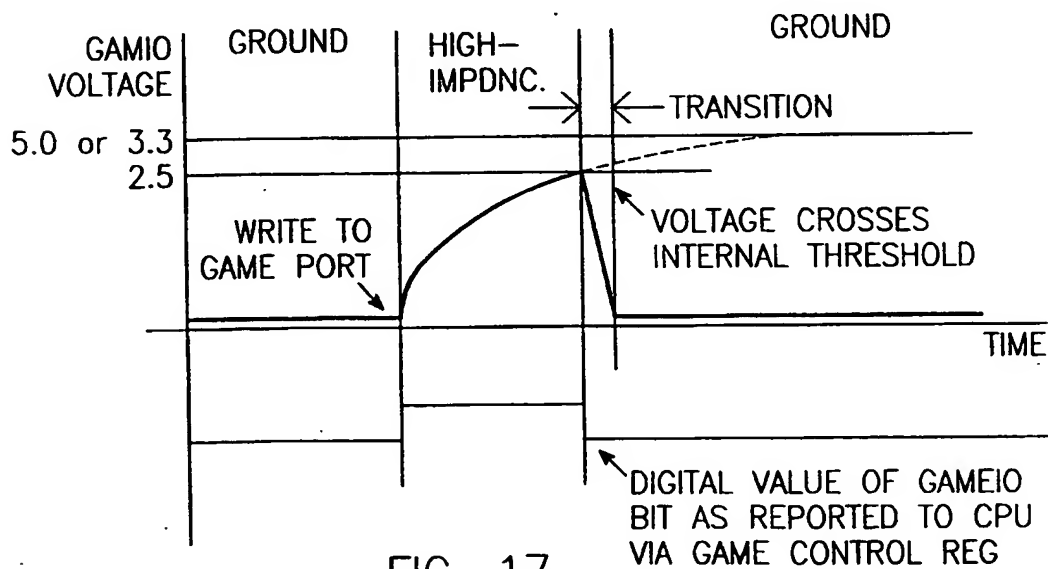


FIG. 17

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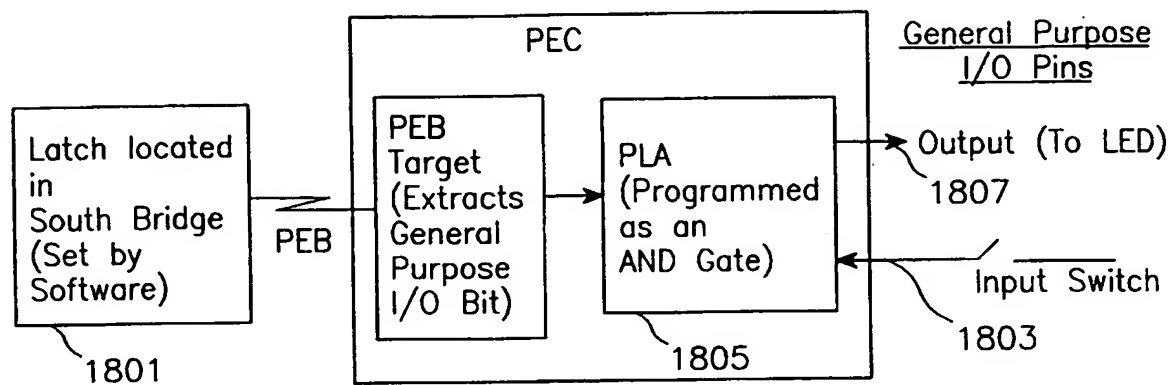


FIG. 18

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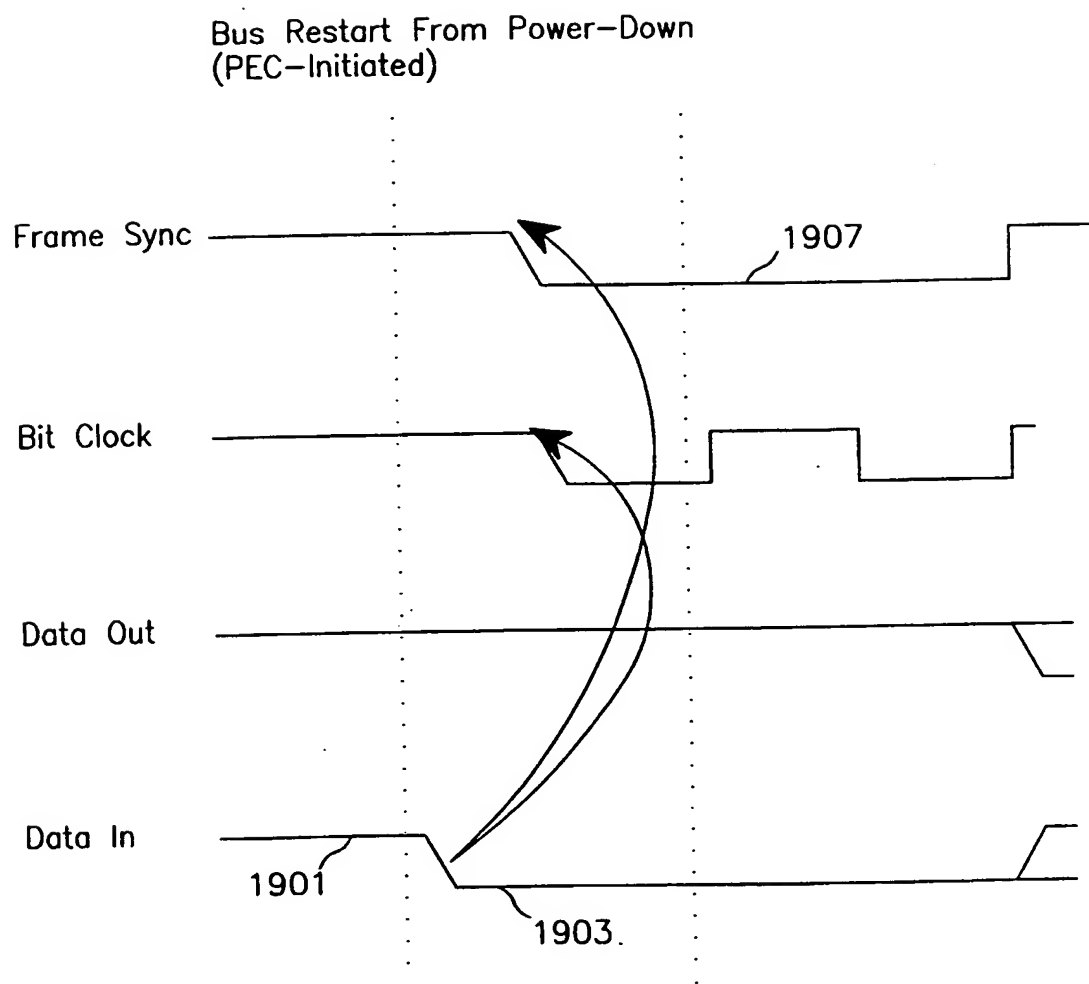


FIG. 19

INTERNATIONAL SEARCH REPORT

Inte. .onal Application No

PCT/US 98/02762

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F13/40

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>FERNALD ET AL: "A System Architecture for Intelligent Implantable Biotelemetry Instruments" PROCEEDINGS OF THE ANNUAL CONFERENCE OF THE IEEE / ENGINEERING IN MEDICINE AND BIOLOGY SOCIETY, vol. 11, 9 - 12 November 1989, SEATTLE, WASHINGTON, US, pages 1411-1412, XP000129472 see page 1411, left-hand column, paragraph 1; figure 1 see page 1411, left-hand column, paragraph 3 see page 1411, right-hand column, paragraph 1 see page 1412, left-hand column, paragraph 1 - right-hand column, paragraph 1; figure 3</p> <p style="text-align: center;">— -/-</p>	1,11,15



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

23 June 1998

Date of mailing of the international search report

01/07/1998

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INTERNATIONAL SEARCH REPORT

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PCT/US 98/02762

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	H. BERNSTEIN: "Gute Bus-Verbindungen: PCI-Chipsets für 46-Bit-Mikroprozessoren" ELEKTRONIK., vol. 43, no. 18, 6 September 1994, MUNCHEN DE, pages 110-115, XP000471349 see page 110, left-hand column, paragraph 1 - page 113, left-hand column, paragraph 1	1,11
A	US 5 455 740 A (BURNS) 3 October 1995 see column 2, line 11 - line 18; figure 1	1,11

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int'l. Application No

PCT/US 98/02762

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 5493476 A	20-02-1996
		US 5605592 A	25-02-1997
		US 5552963 A	03-09-1996
		US 5586009 A	17-12-1996